Thesis for the degree of Doctor of Philosophy

Fundamental Characterization of Low Dimensional Carbon Nanomaterials for 3D Electronics Packaging

Andreas Nylander

Department of Microtechnology and Nanoscience - MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2021

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Andreas Nylander
ISBN 978-91-7905-440-3

Chalmers University of Technology
Department of Microtechnology and Nanoscience - MC2
Electronic Materials and Systems Laboratory
SE–412 96 Göteborg, Sweden
Telephone + 46 (0) 31 – 772 1000

Doktorsavhandlingar vid Chalmers tekniska högskola
ISSN 0346-718X
Ny serie nr 4907

Cover image:
Abstract rendering of the inside of a carbon nanotube that exposes the sp^2 hexagonal lattice that many of the low dimensional carbon nanomaterials have in common.

"There ain't no such thing as a free lunch."
—Robert. A. Heinlein.

Abstract

Transistor miniaturization has over the last half century paved the way for higher value electronics every year along an exponential pace known as 'Moore's law'. Now, as the industry is reaching transistor features that no longer makes economic sense, this way of developing integrated circuits (ICs) is coming to its definitive end. As a solution to this problem, the industry is moving toward higher hanging fruits that can enable larger sets of functionalities and ensuring a sustained performance increase to continue delivering more cost-effective ICs every product cycle. These design strategies beyond Moore's law put emphasis on 3D stacking and heterogeneous integration, which if implemented correctly, will deliver a continued development of ICs for a foreseeable future. However, this way of building semiconductor systems does bring new issues to the table as this generation of devices will place additional demands on materials to be successful.

The international roadmap of devices and systems (IRDS) highlights the need for improved materials to remove bottlenecks in contemporary as well as future systems in terms of thermal dissipation and interconnect performance. For this very purpose, low dimensional carbon nanomaterials such as graphene and carbon nanotubes (CNTs) are suggested as potential candidates due to their superior thermal, electrical and mechanical properties. Therefore, a successful implementation of these materials will ensure a continued performance to cost development of IC devices.

This thesis presents a research study on some fundamental materials growth and reliability aspects of low dimensional carbon based thermal interface materials (TIMs) and interconnects for electronics packaging applications. Novel TIMs and interconnects based on CNT arrays and graphene are fabricated and investigated for their thermal resistance contributions as well electrical performance. The materials are studied and optimized with the support of chemical and structural characterization. Furthermore, a reliability study was performed which found delamination issues in CNT array TIMs due to high strains from thermal expansion mismatches. This study concludes that CNT length is an important factor when designing CNT based systems and the results show that by further interface engineering, reliability can be substantially improved with maintained thermal dissipation and electrical performance. Additionally, a heat treatment study was made that enables improvement of the bulk crystallinity of the materials which will enable even better performance in future applications.

Keywords: : Thermal management, Electrical interconnects. Thermal interface material, Carbon nanotubes, Graphene, Reliability aspects, Heat treatment.

List of Publications

Appended Papers

This thesis is based on the following papers:

Paper A. Current Status and Progress of Organic Functionalization of CNT Based Thermal Interface Materials for Electronics Cooling Applications
Andreas Nylander, Yifeng Fu, Lilei Ye, Johan Liu
2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Sweden, 2017. DOI: 10.1109/NORDPAC.2017.7993188

Paper B. Covalent Anchoring of Carbon Nanotube Based Thermal Interface Materials Using Epoxy Silane Monolayers
Andreas Nylander, Yifeng Fu, Mingliang Huang, Johan Liu
IEEE Transactions on Components, Packaging and Manufacturing Technology. DOI: 10.1109/TCPMT.2018.2863791

Paper C. Reliability Investigation of a Carbon Nanotube Array Thermal Interface Material
Andreas Nylander, Josef Hansson, Majid Kabiri Samani, Christian Chandra Darmawan, Ana Borta Boyon, Laurent Divay, Lilei Ye, Yifeng Fu, Afshin Ziaei and Johan Liu
MDPI Energies, 2019, DOI: 10.3390/en12112080

Paper D. Synthesis of a Graphene Carbon Nanotube Hybrid Film by Joule Self-heating CVD for Thermal Applications
Josef Hansson, Majid Kabiri Samani, **Andreas Nylander**, Lilei Ye, Nan Wang, Torbjörn M.J. Nilsson and Johan Liu
2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, 2018, DOI: 10.1109/ECTC.2018.00369

Paper E. Degradation of Carbon Nanotube Array Thermal Interface Materials Through Thermal Aging: Effects of Bonding, Array Height and Catalyst Oxidation
Andreas Nylander, Josef Hansson, Torbjörn M.J. Nilsson, Lilei Ye, Yifeng Fu and Johan Liu
Accepted, ACS Applied Materials and Interfaces, 2021

Paper F. Multiple growth of graphene from a pre-dissolved carbon source
Andrea Fazi, **Andreas Nylander**, Abdelhafid Zehri, Jie Sun, Per Malmberg, Lilei Ye, Johan Liu and Yifeng Fu
IOP Nanotechnology, 2020, DOI: 10.1088/1361-6528/ab9040

Paper G. RF Properties of Carbon Nanotube / Copper Composite Through Silicon Via Based CPW Structure for 3D Integrated Circuits
Andreas Nylander, Marlene Bonmann, Andrei Vorobiev, Josef Hansson, Nan Wang, Yifeng Fu and Johan Liu
2019 IEEE 14th Nanotechnology Materials and Devices Conference (NMDC), Stockholm, 2019, DOI: 10.1109/nmdc47361.2019.9084012

Paper H. Effects of high temperature treatment of carbon nanotube arrays on graphite: increased crystallinity, anchoring and inter-tube bonding
Josef Hansson, **Andreas Nylander**, Mattias Flygare, Krister Svensson, Lilei Ye, Torbjörn M.J. Nilsson, Yifeng Fu and Johan Liu
IOP Nanotechnology, 2020, DOI: 10.1088/1361-6528/ab9677

Other Contributions

Development of bulk-nanostructuring methods for BiSbTe thermoelectrics
Andreas Nylander, Nikolaos Logothetis, Johan Liu
2016 IMAPS Nordic Conference on Microelectronics Packaging, Norway, 2016.

Embedded Fin-Like Metal/CNT Hybrid Structures for Flexible and Transparent Conductors
Di Jiang, Nan Wang, Michael Edwards, Wei Mu, **Andreas Nylander**, Yifeng Fu, Kjell Jeppson, Johan Liu
Small, Volume 12, Issue 11, 2016, 1521-1527. DOI: 10.1002/smll.201503091

Thermal Conductivity Enhancement of Coaxial Carbon@Boron Nitride Nanotube Arrays
Lin Jing, Majid Kabiri Samani, Bo Liu, Hongling Li, Roland Tay, Siu Hon Tsang, Oliver Cometto, **Andreas Nylander**, Johan Liu, Edwin Hang Tong Teo, Alfred Ling Yoong Tok
ACS Applied Materials & Interfaces, Volume 9, Issue 17, 2017, 14555–14560. DOI: 10.1021/acsami.7b02154

Thermal Reliability Study of Polymer Bonded Carbon Nanotube Array Thermal Interface Materials
Andreas Nylander, Christian Chandra Darmawan, Ana Borta Boyon, Laurent Divay, Majid Kabiri Samani, Mohamad Abo Ras, Julien Fortel, Yifeng Fu, Lilei Ye, Afshin Ziaei and Johan Liu
2018 24rd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Amsterdam, 2018. DOI: 10.1109/Therminic44018.2018

Thermally Conductive and Electrically Insulating PVP/Boron Nitride Composite Films for Heat Spreader
Ya Liu, Nan Wang, Lilei Ye, Abdelhafid Zehri, **Andreas Nylander**, Amos Nkansah, Hongbin Lu and Johan Liu
2019 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Lungby, Denmark, 2018. DOI: 10.23919/NORDPAC.2019.8760352

Graphene-coated copper nanoparticles for thermal conductivity enhancement in water-based nanofluid
Abdelhafid Zehri, **Andreas Nylander**, Lilei Ye and Johan Liu
2019 22nd European Microelectronics and Packaging Conference and Exhibition (EMPC), Pisa, Italy, 2019. DOI: 10.23919/EMPC44848.2019.8951883

Bipolar electrochemical capacitors using double-sided carbon nanotubes on graphite electrodes
Josef Hansson, Qi Li, Andersson Smith, Isaac Zakaria, Torbjörn M.J. Nilsson, **Andreas Nylander**, Lilei Ye, Per Lundgren, Johan Liu and Peter Enoksson
Elsevier Journal of Power Sources, Volume 451, 1 March 2020, 227765, DOI: 10.1016/j.jpowsour.2020.227765

High porosity and light weight graphene foam heat sink and phase change material container for thermal management
Abdelhafid Zehri, Majid Kabiri Samani, Martí Gutierrez Latorre, **Andreas Nylander**, Torbjörn M.J. Nilsson, Yifeng Fu, Nan Wang, Lilei Ye, and Johan Liu
IOP Nanotechnology, Volume 31, Number 42 2020, DOI: 10.1088/1361-6528/aba029

List of Acronyms

ACA	–	Anisotropic Conductive Adhesive
AFM	–	Atomic Force Microscopy
BEOL	–	Back End Of Line
BGA	–	Ball Grid Array
BLT	–	Bondline Thickness
C4	–	Controlled Collapse Chip Connection
CMOS	–	Complementary Metal Oxide Semiconductor
CMP	–	Chemical Mechanical Planarization
CNT	–	Carbon Nanotube
CPU	–	Central Processing Unit
CPW	–	Co-Planar Waveguide
CTE	–	Coefficient of Thermal Expansion
CVD	–	Chemical Vapor Deposition
DI	–	De-Ionized water
DNP	–	Distance to Neutral Point
DRIE	–	Deep Reactive Ion Etching
FEOL	–	Front End Of Line
GLYMO	–	(3-Glycidyloxypropyl)-trimethoxysilane
I/O	–	Input Output
IC	–	Integrated Circuit
ICA	–	Isotropic Conductive Adhesive
IHS	–	Internal Heat Spreader
ITRS	–	International Technology Roadmap for Semiconductors
IRDS	–	International Roadmap of Devices and Systems
MDS	–	Molecular Dynamics Simulation
MEMS	–	Micro-Electro-Mechanical System
MFP	–	Mean Free Path
MPC	–	Molecular Phonon Couplers
PCM	–	Phase Change Material
PEMA	–	Poly(Ethyl Methacrylate)
PGS	–	Pyrolytic Graphite Sheet
PLP	–	Particle Laden Polymer
PPR	–	Pulsed Photothermal Reflectance
PVD	–	Physical Vapor Deposition

SEM	–	Scanning Electron Microscope
SIMS	–	Secondary Ion Mass Spectrometry
SiP	–	System in a Package
TAB	–	Tape-Automated Bonding
TCA	–	Thermally Conductive Adhesive
TDP	–	Thermal Design Power
TEM	–	Transmission Electron Microscopy
TIM	–	Thermal Interface Material
TSV	–	Through Silicon Via
VDOS	–	Vibrational Density Of States
VLSI	–	Very Large Scale Integration
WB	–	Wire Bonding
XPS	–	X-ray Photoelectron Spectroscopy

Contents

Chapter 1

Introduction

1.1 Background

Miniturization of integrated circuits (ICs) based on complementary metal oxide semiconductor (CMOS) transistors has over the last 70 years developed in an exponential pace, resulting in additional computational power at affordable rates every consecutive year. This trend was already predicted and coined as 'Moore's Law' in 1965 by Gordon Moore [1], who at the time was working at Fairchild Semiconductor, later a co-founder of Intel. 'Moore's Law' states that the number of transistors possible on a given area in very large scale integration (VLSI) processes would double every 12 - 18 months. This way, a cost to performance development has been possible that follows the same trend. Thus, the semiconductor industry has fueled the global economic growth by motivating the development of increased performance of affordable devices every couple of years [2].

Heat in electronic systems is concentrated at high performance components as the thermal dissipation of ICs directly correspond to the power consumption of each component. This is an issue both at the component and board levels of packaging as the heat from hot spots generated will be dissipated out through the system and cause reliability concerns [3]. The thermal dissipation needs have therefore steadily increased due to processing units being developed with increased transistor densities and performance each year along the predicted pace [1]. The power dissipation of a transistor can be expressed as [4]:

$$P = CV^2 f \tag{1.1}$$

Where P is the consumed power in the transistor, C is the dynamic capacitance, V is the transistor voltage and f is the transistor frequency. Since the transistor frequency is proportional to the transistor voltage, the power can be expressed as the cube of the transistor frequency [5]:

$$P \propto f^3 \tag{1.2}$$

This cubic relation between power consumption and transistor frequency results in a limit, called the thermal barrier, where thermal management solutions no longer

can dissipate the generated heat to maintain an acceptable junction temperature. The semiconductor development reached the thermal barrier around year 2000 when the hot spot temperatures became too difficult to handle. Therefore, developers reduced the overall clock frequency in favor of multiple core designs that allowed workloads to be split into several threads which successfully continued the performance to cost development according to 'Moore's Law' [6]. This strategy solved the rampant thermal issues for a while but transistor miniaturisation would still continue persisting power density increments, due to the same amount of power being dissipated on a smaller area. Figure 1.1 highlights the development of Intel processors in terms of thermal design power (TDP), cores, transistors and frequency over the last 50 years.

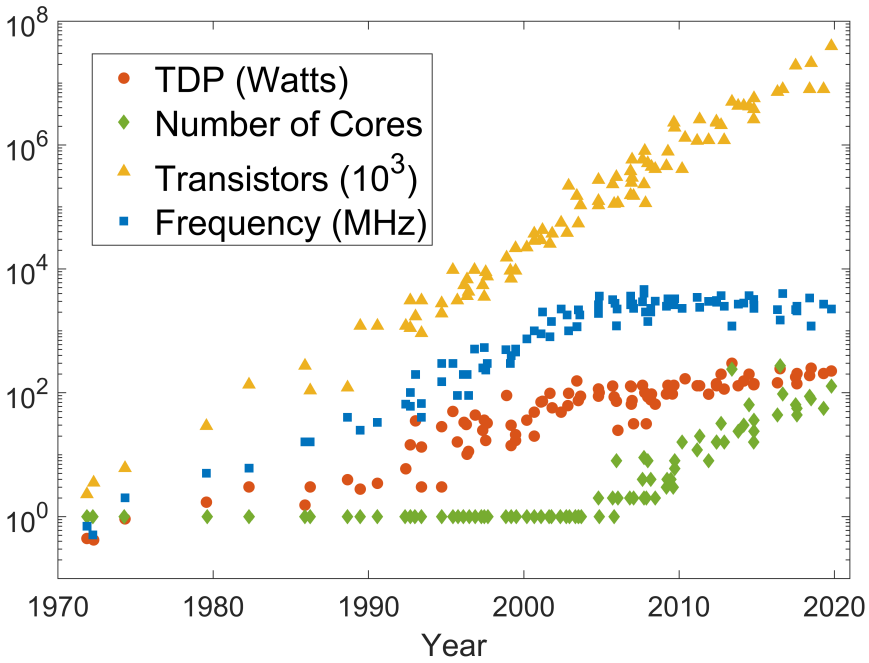


Figure 1.1: Development of consumer CPUs between 1970 to 2020. Original data up to 2010 collected by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten. Data between 2010 and 2020 collected by K. Rupp [7]. Adapted under CC BY 4.0.

The miniaturization of transistors has continued since the introduction of multiple core central processing units (CPUs) and has now reached dimensions that challenge the physical limitations where quantum effects are becoming noticeable. These effects manifest themselves mainly in terms of leakage currents and signal noise which obstructs the operation of CMOS devices [8]. As such, traditional transistor scaling is reaching its end and the industry is trying to find new ways forward. According to the IRDS 2020, future generations of CMOS devices will be developed using design concepts like 3D stacking and heterogeneous integration [9]. These new concepts will aid the industry to reach higher performance and increased levels of integration at lower fabrication costs. A successful implementation would therefore deliver 'More Moore' and continue the traditional miniaturization progression over

a foreseeable future. However, this paradigm shift will require improved packaging solutions both in terms of thermal management and for interconnects to ensure reliability of 3D packaged IC systems.

1.2 Thermal Management by Thermal Interface Materials

Thermal management became a vital part of electronics packaging in the early '90s with the introduction of the ball grid array (BGA) package which allowed higher performance levels than what previously had been possible [10]. This led to higher operation temperatures and resulted in device failures as a consequence [11, 12]. To counter the increased operation temperatures, new passive cooling solutions like internal heat spreaders (IHS), heat sinks and thermal interface materials (TIMs) were developed and built around the active Si chip. A thermal package like this could in turn be coupled with active cooling solutions based on air or water. A thermal package including standard passive cooling components is illustrated in Figure 1.2.

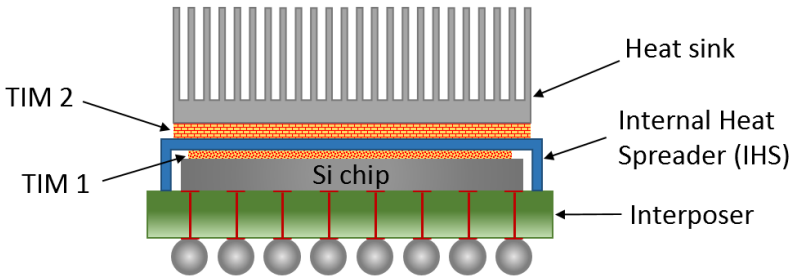


Figure 1.2: Common thermal package built around an interposer structure and a CPU chip. The chip is connected to an IHS and in turn to a heatsink using TIMs to alleviate the CPU from excessive thermal build-up.

Due to the impossibility of attaining surfaces with atomic flatness, gaps will always form in the interface between two materials [13]. These gaps will constrict thermal conduction pathways over the interface by isolating a large fraction of the total interface area with air pockets. This severely impedes the thermal dissipation over the interface as the air gaps effectively acts like a thermos. This issue can be circumvented using TIMs to connect the processor to an IHS and subsequently the IHS to a heat sink. A conformable material with higher thermal conductivity than air can be used to fill out the gaps in the interface and reduce the thermal resistance in the interface. Unfortunately, performance requirements on TIM1 solutions have increased in relation to TIM2 and active cooling combined. The relative thermal resistance contribution that TIM1 needs to alleviate grew from 50% to 85% between the 90 and 35 nm process nodes [14]. This means that TIM1 is a major bottleneck that needs attention in order to ensure future performance increments in CMOS devices.

According to Fourier's law, $Q = \frac{1}{R}\Delta T$, thermal resistance R is a measure of how well a material can resist a heat flow Q, which in turn gives rise to a temperature drop ΔT. In the same way, thermal boundary resistance (kapitza resistance) is a measure of the thermal resistance across an interface. The thermal resistance over a TIM, R_{th} can thus be expressed according to Equation 1.3.

$$R_{th} = R_{C1} + \frac{BLT}{\kappa_{TIM}} + R_{C2} \tag{1.3}$$

The total resistance over a TIM is expanded into two different types of contributions: The thermal boundary resistances R_{C1} and R_{C2} on either side of the interface and the bulk thermal interface resistance R_{TIM} originating from the TIM itself. R_{TIM} can in turn be described by the fraction of the bond line thickness (BLT) and κ_{TIM}, which is the thermal conductivity of the material. An illustration of a TIM applied between two surfaces along with the TIM working principle is illustrated in Figure 1.3.

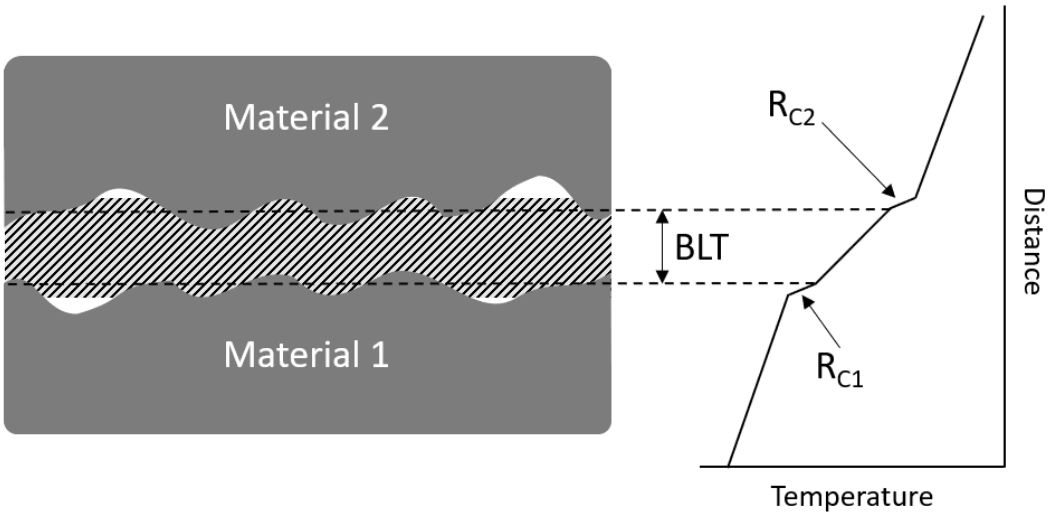


Figure 1.3: Thermal interface with a TIM applied in between two surfaces. The BLT of the TIM is marked together with the thermal boundary resistance contributions R_{C1} and R_{C2}.

To achieve a high performance TIM design, the origins of the thermal contact resistance that arises between two surfaces must be understood. This was illustrated by Yovanovich et al. in the thermal contact resistance triad [15]. The triad highlights the interplay between surface topology in an interface (geometry), mechanical conformability and thermal performance and is illustrated in Figure 1.4. Therefore, an ideal TIM should have a high thermal conductivity coupled with an ability to conform to the surface topology found in the interface. That way, an optimal reduction of the thermal boundary resistance can be achieved. Furthermore, mechanical compliance is also beneficial for the TIM to adapt under stress, this is to compensate for CTE mismatches that otherwise can damage the interface.

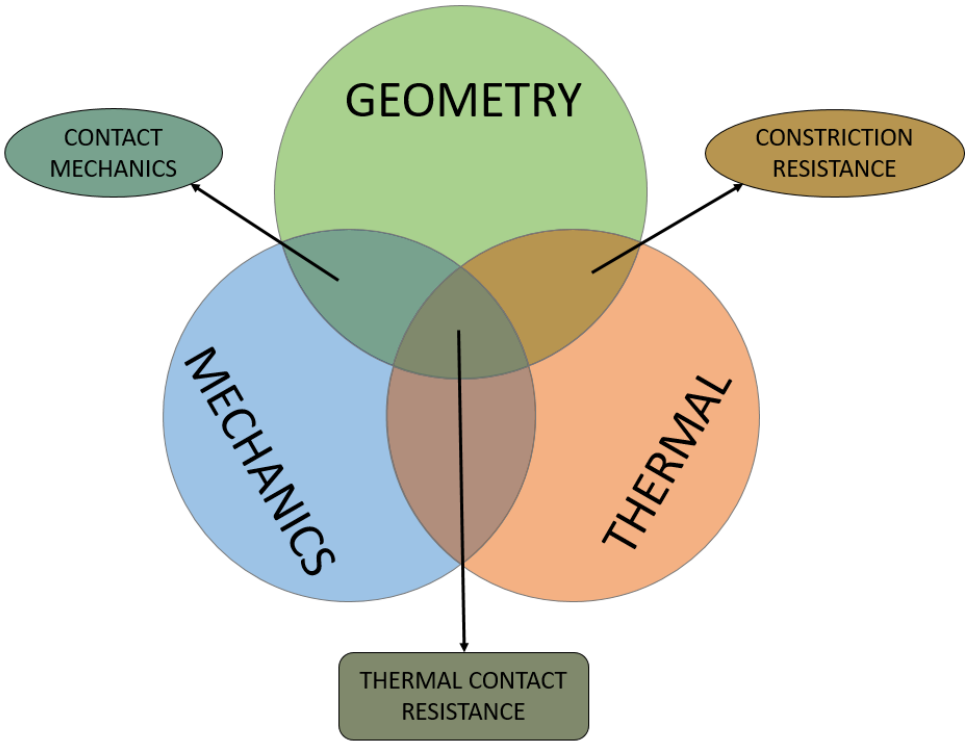


Figure 1.4: Thermal contact resistance triad that showcases the interplay between geometry, mechanical and thermal properties of a thermal contact.

Commercially available TIMs today are either based on particle laden polymer (PLP) or solder designs. PLP based TIMs are composed of a polymer matrix loaded with particles of high thermal conductivity. This enables these types of TIMs to possess a high level of conformability with decent performance, provided that the particle loading surpasses the percolation limit [13]. Thermal grease is a basic type of PLPs without any adhesive functionality. This keeps the interface mechanically decoupled while decreasing the thermal interface resistance. Thermally conductive adhesive (TCA) is another type of PLP TIM that can be used to mechanically couple the interface, this locks the components in position with a low level of ductility that can absorb stress. Although PLP based TIMs offer a high level of reliability, the thermal conductivity is relatively low. Solder based TIMs on the other hand offer a superior thermal conductivity compared to PLP TIMs [14]. Unfortunately, the rigid mechanical nature of metallic systems like solder suffers from reliability issues that can crack the interface. Such cracks will continue to propagate through the entire solder phase and result in imminent system failure. Other variants of TIMs exist on the market as well. These are mainly in form of phase change materials (PCM) and PLP based thermal pads. PCMs are often used as a thermal buffer in applications where the thermal load is cycled in intervals instead of maintaining a constant power output [16]. Thermal pads are designed to conform well under pressure and are reusable at the expense of high thermal resistance. This type of TIM does not suffer from 'pump out' effects unlike both thermal grease and PCMs which is beneficial from a reliability point of view [17, 18]. These different commercially available TIMs are listed in Table 1.1 for a quick overview of the typical thermal resistance offered.

Table 1.1: Different TIM categories with typical expected performance, from ref. [19]

Thermal interface material type	**Typical Thermal Interface Resistance (mm^2K/W)**
Thermal Grease	10 - 200
Thermal pad	100 - 300
Thermally Conductive Adhesive	50 - 200
Phase Change Material	30 - 70
Solder	<5

Currently available TIM solutions always require the end user to compromise between performance and reliability. Therefore, new solutions with combined performance and reliability are sought after as the thermal dissipation requirements continue to increase.

1.3 Interconnect Technology in Electronics

Interconnect design for microelectronic systems and VLSI is a large part of the electronics packaging discipline as interconnects have become one of the dominating bottlenecks determining the resulting performance [20]. Interconnects are primarily used for two purposes: signal routing and power distribution [3]. By careful design of the IC package, functionality, performance, power efficiency and reliability can be reached. However, additional demands are placed on interconnect designs as the technology scales to smaller and more advanced device geometries.

A microelectronic package houses I/O (input output) interconnections at different levels in the system [3]. The on-chip level, which traditionally is denoted as level 0, concerns the interconnects patterned directly on the die, as illustrated in Figure 1.5a. These interconnects are either designed as local, intermediate or global interconnects [21]. Local interconnects are used between gates in short proximity. Intermediate interconnects are used to facilitate signal routing between logical blocks. Finally, global interconnects are used to carry clock signals and power, which also means that they need to be larger in size and length compared to the local and intermediate interconnects.

The next level of packaging deals with connections between die and package and is referred to as packaging level 1. Standard methods for packaging at this level are wire bonding and flip chip (controlled collapse chip connection, C4) techniques, as illustrated in Figure 1.5b and 1.5c. Connections by wire bonding can be made using a specialized machine to attach a metal wire to a pad, either by wedge or ball bonding [22, 23]. In this way, contacts can be formed one by one in series along the periphery of the chip. The more modern flip chip technique relies on having all the

connectors already formed on the chip as solder micro bumps. That way, all the interconnects can be established in parallel using a flip chip bonder machine. The advantages of flip chip compared to wire bonding is that I/Os can be packed over the whole area instead of only along the periphery of the chip and that the interconnect length can be significantly reduced. Additionally, tape-assisted bonding (TAB) also exists but has largely been replaced by flip chip as it offers the same advantages as flip chip over wire bonding with additional drawbacks in terms of specialized tools and application-specific restrictions [3].

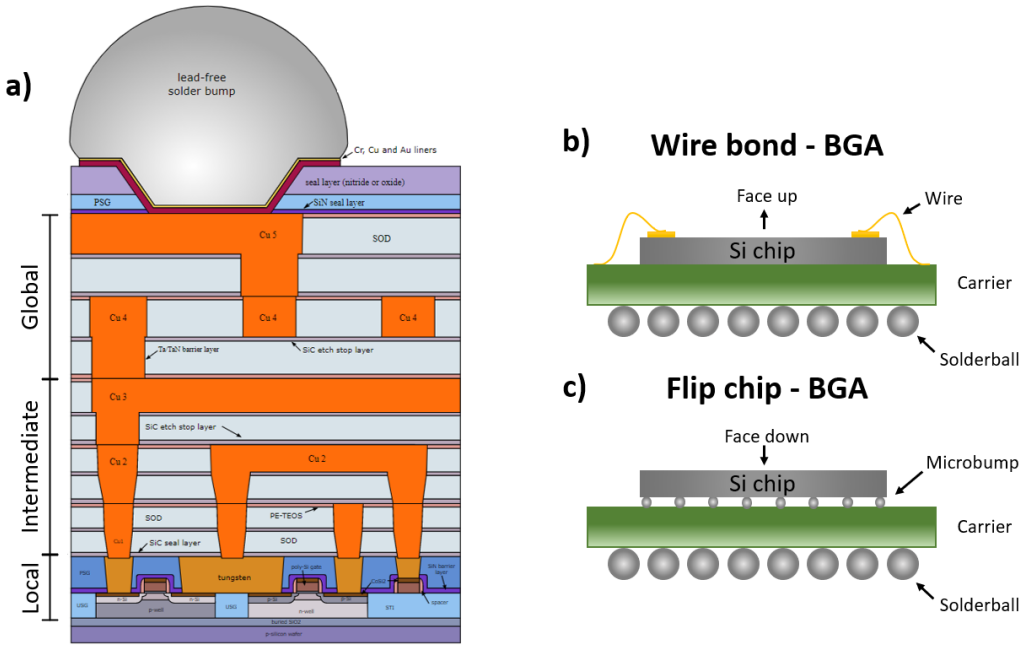


Figure 1.5: Different types of interconnects both 'on-chip' and chip to board levels. a) through section of the back end of line (BEOL) and front end of line (FEOL) layers of a modern VLSI device which highlights the local, intermediate and global levels of interconnects. Original work by Cepheiden [24], adapted under CC-BY-SA-3.0. b) BGA package connected to a chip using wire bonding. c) BGA package connected to a chip using flip chip bonding.

As VLSI node designs used for CMOS devices are reaching beyond 5 nm [25], new solutions are required in order to continue increasing the transistor density [26]. By stacking dies vertically, developers will have access to a new dimension for further transistor density scaling. Stacked chip assemblies can be constructed in a multitude of ways with the 2.5D and 3D system in a package (SiP) designs being the easiest to engineer as they are built around ordinary stacked dies. Monolithic 3D ICs are on the other end of the difficulty spectrum and utilizes the entire chip volume for transistors. Two types of 3D stacked SiPs are illustrated in Figure 1.6. The first is connected to package using wire bonded connections die to package, as illustrated in Figure 1.6b. The other is constructed using flip chip to stack the dies in complement with through silicon vias (TSVs) that routes signals through the levels of dies [3], as illustrated in Figure 1.6c. In other words, TSV technology can reduce

the interconnect length used to connect dies to package and at the same time allow higher density of I/Os. Additionally, this would allow the stack to be made up of dies with equal area available for transistors. TSV type interconnects are therefore seen as one of the key enabling technologies to develop in order to realise true 3D integration for the next generation of IC devices [9].

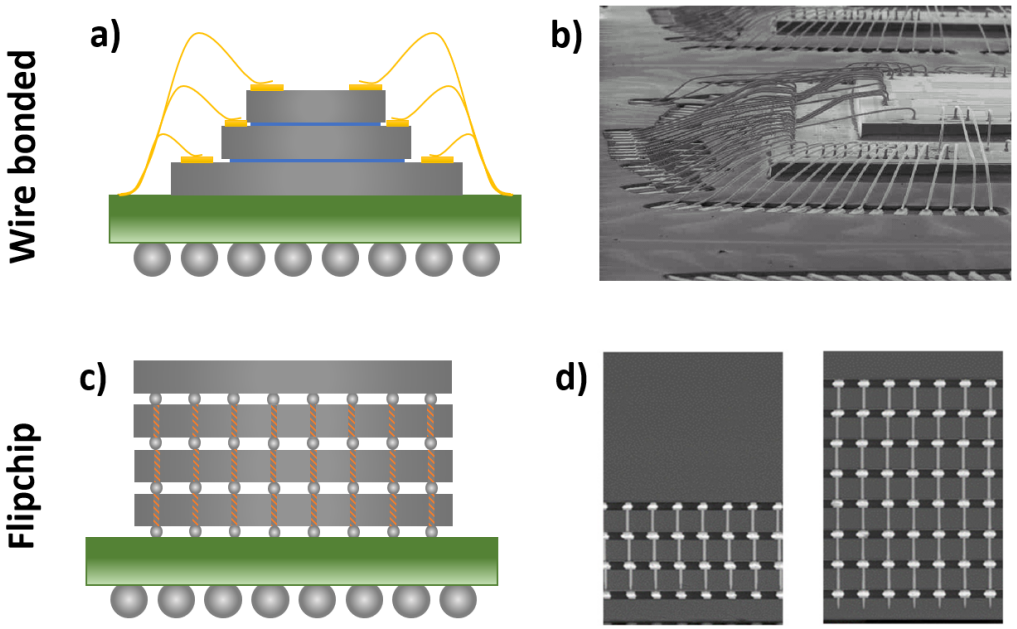


Figure 1.6: 3D packages achieved with: a) wire bonding and c) flip chip and TSVs. Examples of the two different 3D packages: b) wire bonded 3D SiP and d) 4 and 8 layered DRAM packaged through flip chip. Adapted from [27] and [28].

There are many factors that affect the end performance of electrical interconnects in terms of reliability, power consumption and signal delays. The reliability aspect of an interconnect is both CTE mismatch induced strains, as previously mentioned, as well as electromigration. The electromigration issue occurs when the current density that is fed trough the interconnect increases along the scaling of device design. The interconnect material therefore requires an ampacity (current carrying capacity) that is greater than the current density in order to ensure long term reliability. Power consumption of the device is highly dependent of its total resistance according to $V = I \cdot R$ and will increase as the feature size of the interconnects scales. At the same time, signal delays arise due to the RC effect which is the product of the resistance and capacitance associated with the interconnect conductor [20]. The signal delay from interconnects between gates in IC devices has increased from 15 % up to 80 % over the last 40 years as a result of the shrinking feature size [29].

The current industry standard for interconnects on both packaging level 0 and 1 is Cu due to the excellent electrical, thermal and mechanical properties it offers as well as the low associated manufacturing costs [30]. As such, the performance of interconnects will be dependent on the inherent properties of Cu and geometries

used for these interconnects. By switching Cu wire bonding for Cu TSVs for 3D packaging solution on packaging level 1, large resistivity and capacitive improvements can be made which would improve the performance of devices. Unfortunatly, Cu based TSVs that are used in contemporary industry processes are susceptible to CTE induced thermal reliability issues that arise between the Si die and the Cu filling in the via [31]. Therefore, TSVs have most prominently been featured in memory stacks and micro-electrical-mechanical systems (MEMS) and been largely absent from high effect devices like ICs [32]. Packaging level 0 interconnects are, on the other hand, designed with dimensions related to the fabrication process node. This means that VLSI scaling will result in an escalation of resistivity, capacitance, RF signal losses and electromigration as the development pushes the physical dimensions of interconnects down to and beyond the mean free path (MFP) of Cu [33–36]. However, Cu is still projected to remain as the preferred solution at least until 2021, after which a replacement should be found [9].

1.4 Low Dimensional Carbon Materials

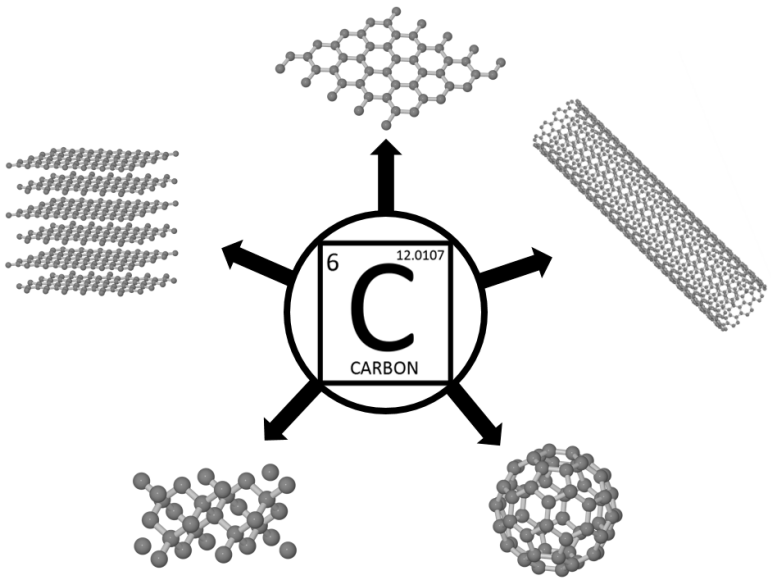


Figure 1.7: Carbon can assume many possible allotrope configurations. The chemical structure is presented for: graphene (top), carbon nanotube, C60 Fullerene, diamond and graphite.

Element number 6 in the periodic table, otherwise referred to as carbon, is one of the most versatile chemical components known to mankind. Carbon is the foundation of all organic chemistry due to its ability to form double and triple bonds with its four valence electrons and the property of self-linkage (i.e. catenation). This allows carbon to arrange itself into longer chains in many varieties and allows carbon to exist in an unprecedented amount of complex molecules together with other elements. Carbon can also exist in a number of solid forms by itself, this by altering the electron

configuration and is referred to as allotropy. Five common allotropes: graphite, diamond, Buckminsterfullerene C_{60}, graphene and carbon nanotubes (CNT), are illustrated in Figure 1.7.

The carbon atom in its normal form consists of a nucleus with 6 neutrons and 6 protons, as well as 6 electrons. Out of these, 4 are counted as valence electrons. Valence electrons are the electrons that exist in the outer shell of the atom and are available to form bonds with other atoms (2s and 2p in the case of carbon). The electron configuration of an atom is described by assigning each of the electrons to an orbital and spin state. In a nutshell, the orbital is a way to describe a space where it is likely to find the electron at any given time (with about 95% probability, it can however exist anywhere in the universe). Spin is a representation of the angular momentum of an electron and can either be up or down which enables each orbital to house 2 electrons. The ground state of carbon is illustrated in Figure 1.8 and can be written $1s^2 2s^2 2p^2$. This means that carbon, aside from the inner 1s shell, has 2 electrons in the 2s orbital and 1 electron each in the $2p_x$ and $2p_y$ shells. [37]

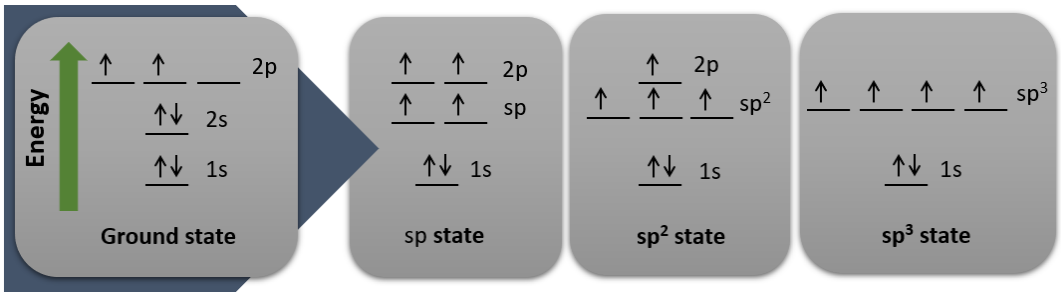


Figure 1.8: Electron configuration of carbon in its ground state compared to the hybridized sp, sp^2 and sp^3 states.

The orbitals can also combine and find new energy levels called hybridized states and these are denoted sp, sp^2 and sp^3, seen in Figure 1.8. As covalent bonding is based on orbital overlap, these hybridized states will also determine how atoms can form larger structures. The difference between the states is how many of the valance orbitals that combines in the hybridization. This is the key factor that will determine the final shape of the hybridized orbitals, as illustrated in Figure 1.9. In the case of the sp^3 hybridization, all valence orbitals contribute which results in a 3D tetrahedron with 105 degrees separation. For the sp and sp^2 hybridizations only one and two 2p orbitals are left which results in a 1D linear 180 degree shape and 2D planar shape with 120 degree separation respectively. [37]

When two hybridized orbitals overlap they form a σ orbital and this is regarded as a covalent bond. The unhybridized 2p orbitals in the case of the sp and sp^2 configurations can also contribute to form bonds. These are positioned out-of-plane to the hybridized orbitals and when two of these are positioned side by side they form a π orbital. A π orbital together with a σ orbital forms a double covalent bond,

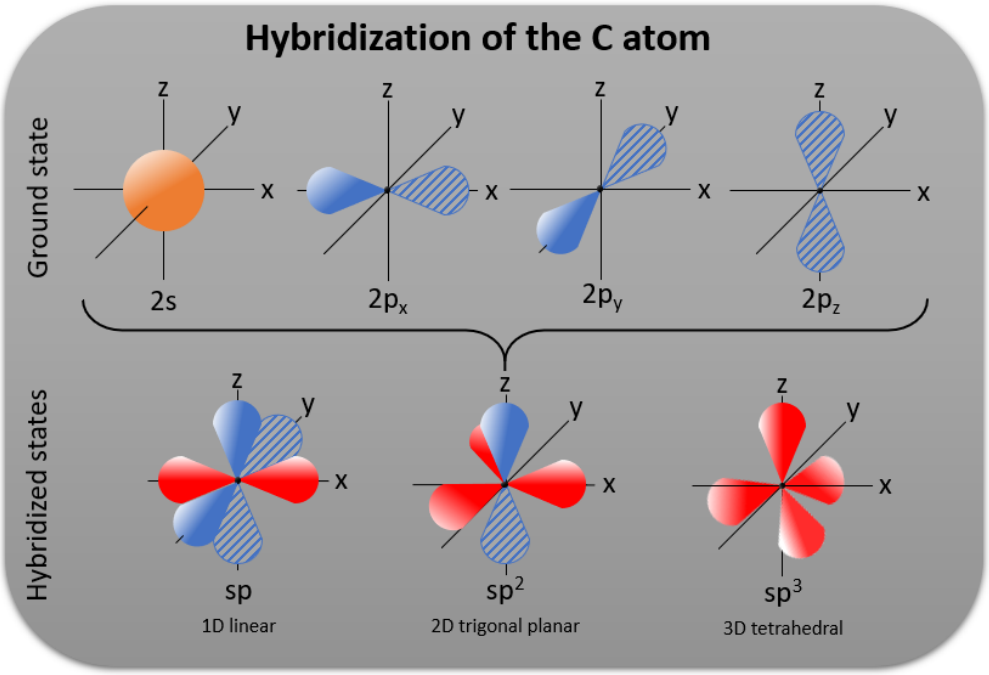


Figure 1.9: Visual representation of the orbital ground state configuration associated with the carbon atom together with the three hybridized states that enables carbon to form different geometries.

and two π and one σ forms a triple covalent bond. The addition of one or two π orbitals makes the bond stiff, in contrast to single covalent bonds that are free to rotate around its own axis. These are the differences that generate 3D diamond, 2D sheets of graphene as well as hydrocarbon chain structures. Graphite is composed of several sheets of graphene stacked on each other with van der Waals forces. The van der Waals force originates from the stacked out-of-plane π-orbitals which also makes it much weaker than the covalent counterpart. Graphite is for that reason weak between the layers which is a suitable trait for many applications like lubricants and pencils. The sp^3 bonded carbon in diamond on the other hand makes it one of the hardest known materials and is therefore suitable for use in drills.

Low dimensional materials are defined as having one, or more, dimensions with a size equal to or smaller than 100 nm [38]. At this length scale, properties of the material will be directly linked to the size. Examples of low dimensional carbon allotropes are: 2D graphene with mono to few layers, single- double- and multiwalled 1D carbon nanotubes, as well as the 0D fullerene which is a ball of hexagonal carbon.

The 2D structure of graphene displays a number of interesting properties as a result of the sp^2 hybridization and lattice structure [39, 40]. Among them are the unusually high electron mobility [41] and electrical conductivity [42]. The electron carrier density of graphene is relatively low which makes phonons the majority carrier for thermal transport. Phonons are quasi particles that represents the potential for

vibrational propagation and these modes will determine the acoustic, optical and thermal properties of a material [43, 44]. The structure of graphene with its strong sp^2 bonds between the relatively light carbon atoms results in an extreme thermal conductivity [45]. Graphene also displays excellent mechanical properties [46, 47] and possesses low optical absorption [48]. This makes graphene interesting for a large set of different applications ranging from electronics, thermal management, construction to name a few. However, the performance of graphene is directly affected once it no longer exist in a free-standing state since many of the desired properties of graphene originate from the out-of-plane π orbitals or the phononic modes.

The CNT, on the other hand, is a 1D tube derivative of graphene and is illustrated in Figure 1.10. CNTs therefore shares many of the unique properties originating from the crystal lattice structure. The CNT is notable for having been predicted to possess the highest thermal conductivity of any known solid (with the exception of graphene) [49], a theoretic electronic current density of 1000 times that of copper [50] and has been measured to possess a mechanical modulus of elasticity that is one order of magnitude higher than steel [51].

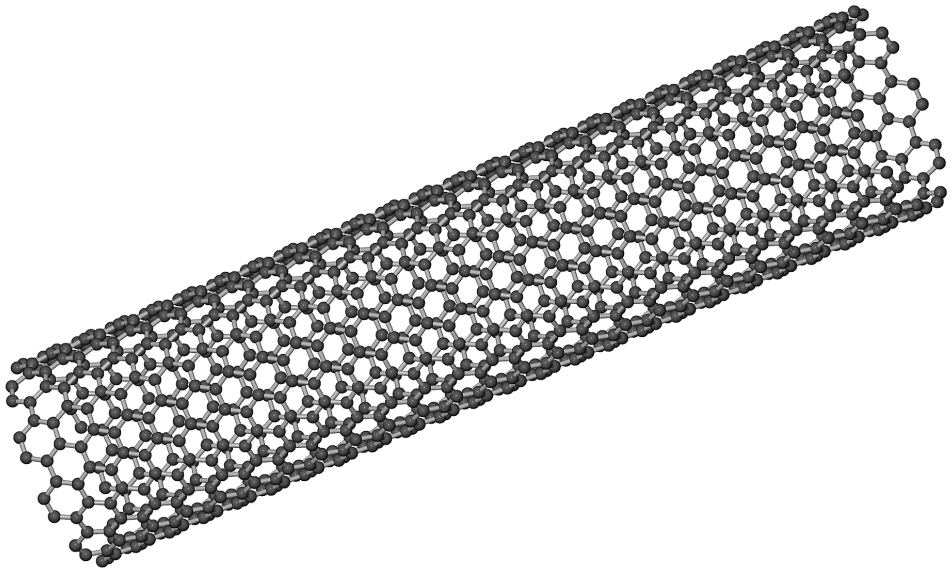


Figure 1.10: Structure of a single walled carbon nanotube.

There are many variants of CNTs where the geometrical configuration can alter physical characteristics of the material. These configurations includes the number of walls, length, diameter, tube alignment and chirality. The electronic nature of a CNT tube is determined by the chirality, i.e. rolling angle, assuming the tube being composed of a rolled graphene sheet. As a consequence, this decides if the tube is of semiconducting or metallic nature [52]. In multi-walled CNTs there are multiple shells present in the tube structure and will as a result always be metallic in nature. Metallic single walled and multi walled CNT have empirically been measured to possess a thermal conductivity of up to 3500 W/mK [53] and 3000 W/mK [54]

respectively, which is 9 and 7 times higher than copper. The metallic single walled CNT has been found to possess an electrical conductivity of 4 x 10^9 A/cm^2 [50]. Since the diameter of CNTs is measured in the nanometer range, they also possess a high surface area to volume ratio. All of these unique characteristics makes CNTs attractive alternatives for a range of different applications and industries, including medical, construction and electronics [55].

Both graphene and CNTs can be synthesised using the chemical vapour deposition (CVD) technique. The materials are manufactured by letting carbonous precursor gases like acetylene or methane react with a catalyst in a controlled manner. Graphene uses a foil of Cu or Ni that the carbon can dissolve into and subsequently diffuse out of as graphene layers [56]. On the other hand, CNTs relies on nanostructured iron catalyst particles that carbon can grow out of in a forest like fashion. This creates tubes stretching vertically from the catalyst nucleation site on the growth substrate and end with a dome shaped cap [57]. This material is commonly referred to as a vertically aligned CNT array and is illustrated in Figure 1.11.

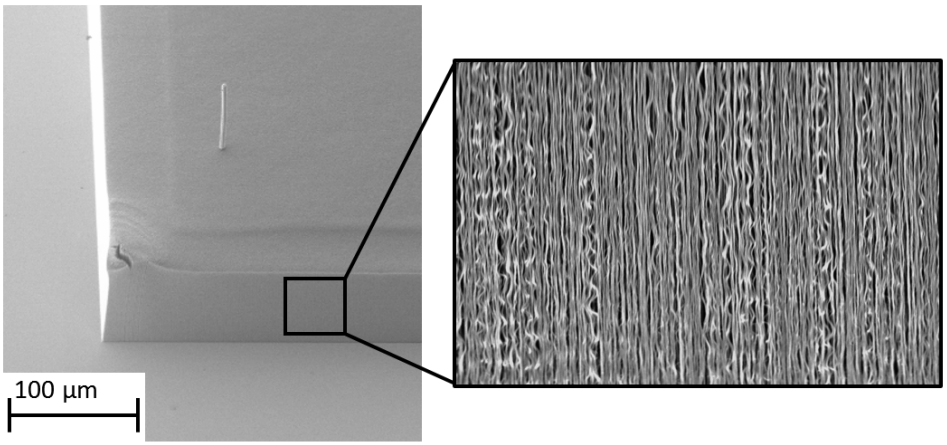


Figure 1.11: Grown CNT array using the CVD method. As seen, the CNTs are aligned in an upwards direction forming a forest like structure of uniform height. Sometimes, anomalous growth can be witnessed resulting in much longer CNTs in a small area of the array.

1.5 This Thesis

The work presented in this thesis deals with the fabrication and characterization of CNT and graphene-based materials for electronics packaging applications. The materials are applied as thermal management and interconnect solutions with the intention to remove bottlenecks in contemporary as well as future devices.

The thesis is divided into four main parts. Chapter 2 deals with CNT array TIMs and starts with a review from Paper A. This review explores the different organic functionalization methods found in literature and the findings are followed by experimental studies on three different types of CNT array TIMs. These are: a self assembly based functionalization technique from Paper B, a polymer bonding approach from Paper C and a double sided graphite/CNT interposer structure from Paper D. The chapter covers the fabrication and characterization details for each of the different CNT array TIMs. Chapter 3 investigates the reliability of CNT array type systems as a continuation of the conclusions from Chapter 2. A systematic study by accelerated aging is presented based on Paper C and E which investigate array length dependence, CTE mismatch considerations and a chemical analysis of the CNT catalyst. Chapter 4 concerns carbon based interconnects for electronic packaging. Two different types of interconnects are explored. The first is based on Paper F and presents a CVD synthesis method on NiCu foils for horizontal graphene interconnects. The second is based on Paper G and explores a Cu/CNT composite structure for use as vertical TSV interconnects. The last main part of the thesis, Chapter 5, presents an experimental high temperature heat treatment for CNT arrays from Paper H. A CNT array grown on a graphite film is analysed after annealing at 3000°C for structural changes, crystallinity, alignment and chemical composition.

The thesis is concluded by outlining future directions in Chapter 6 and discusses how the different research tracks can be developed further for applications in electronics packaging. Finally, Chapter 7 presents a brief summary of the appended papers.

Chapter 2

Carbon Nanotube Array Thermal Interface Materials

With their high thermal conductivity [58] and an excellent mechanical compliance [59], CNTs are seen as a textbook candidate to be used as TIMs for thermal management in accordance with the thermal contact resistance triad illustrated in Figure 1.4. By growing vertically aligned CNTs in arrays by the CVD method, CNT carpets can be obtained and can be used as TIMs for thermal management. This type of TIM is referred to as the CNT array TIM and is bonded between two surfaces for enhanced heat dissipation. This structure is applied in order to allow each of the CNT to span the whole distance between one surface to the other and thereby providing heat conduction pathways as illustrated in Figure 2.1. However, this technology is still not mature enough for an industry adoption and there are still difficulties to be solved to develop processes and analysis methods required for reliable CNT array TIM production.

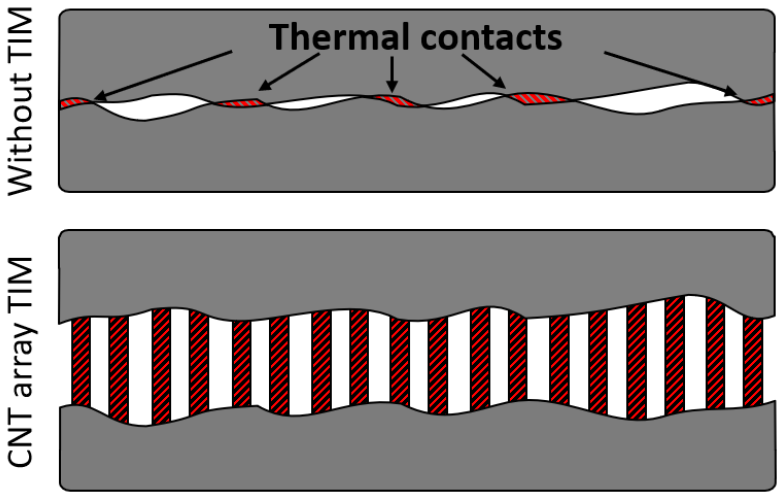


Figure 2.1: Top and bottom figures depicts thermal contacts without the use of a TIM solution and an interface connected through a CNT array TIM respectively. Diagonal stripes represents thermal pathways in each of the interfaces.

This chapter will cover synthesis of CNTs, TIM design and a review of bonding strategies found in literature. These findings are then followed with three of my own approaches to fabricate CNT array TIMs. The chapter summarizes the work presented in Paper A, B, C and D.

2.1 CNT Synthesis and TIM Fabrication

Due to the good alignment of CVD synthesised CNTs, the array structure obtained from CVD growth is well suited for TIM applications where heat needs to be transported from one surface to another [60]. Samples used for CVD based CNT growth consists of a barrier and a catalyst layer on top of a substrate. These materials are commonly prepared using physical vapor deposition (PVD) techniques, more specifically, electron beam evaporation. The catalyst material is chosen for its ability to catalyse hydrocarbons and carbon diffusivity; Fe, Co and Ni are commonly used for this purpose [61–64]. The barrier layer serves two purposes, limiting the catalyst/substrate interaction as well as providing a surface energy that differs from that of the catalyst layer [65]. Surface energy is a measure of the inherent intramolecular tension that was formed during the creation of the surface. By creating a barrier/catalyst interface with enough surface tension will force the catalyst to dewet from the barrier layer and thus divide itself into smaller half spheres during annealing [66, 67]. This mechanism is responsible for the resulting diameter of CNTs as well as the array density. A common choice for the barrier layer is alumina, although quartz, silicon carbide, silica and magnesium oxide among others have been reported to work as well [68]. A typical and reoccurring sample configuration used in this thesis for CNT array growth is silicon substrates with native oxide remaining, covered by a 10 nm thick alumina barrier layer and a 1 nm thick Fe catalyst layer. [68]

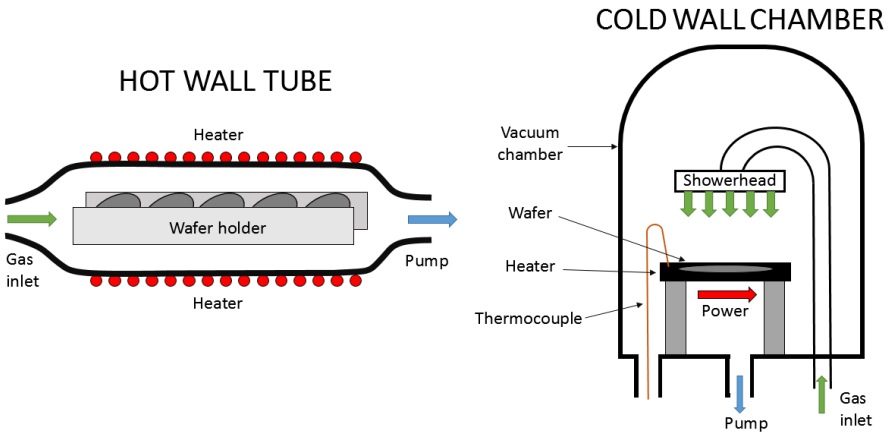


Figure 2.2: Working principles of the hot wall and cold wall CVD systems. Hot wall reactors relies on a uniform heating over the entire chamber which produces reliable process conditions. Cold wall reactors in contrast utilize a localized heater that reduce process time and offers better economy for small scale production.

The CVD process in its simplest form is a chamber that can control pressure, temperature and supply of different gases. Depending on the heater configuration, the process can either be a hot wall CVD or a cold wall CVD as illustrated in Figure 2.2. The hot wall system can achieve a uniform temperature distribution by heating the entire reactor volume, thus providing a large production capacity at the expense of long process times. In contrast, the cold wall system utilises a joule effect heater that results in shorter process times together with production capacity limited to the heater surface area. Both hot wall and the cold wall CVD systems are illustrated in Figure 2.2.

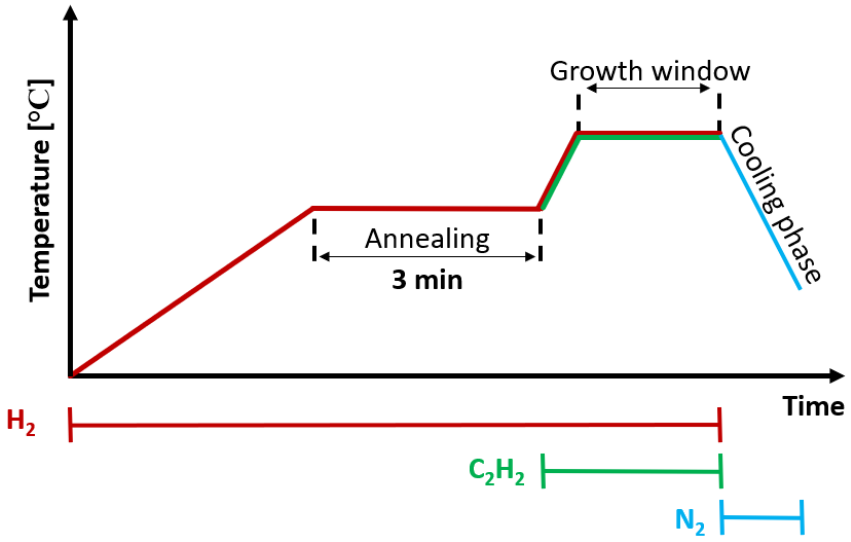


Figure 2.3: Diagram of the typical process when growing CNT arrays using H_2, C_2H_2 and N_2 process gases.

A CVD process for CNT growth on silicon/alumina/Fe systems is depicted in Figure 2.3. The growth process begins with samples inside the growth chamber under vacuum. The temperature ramps at a controlled pace under H_2 atmosphere to the chosen annealing temperature and maintains it long enough to soak. The annealing temperature is usually set to 500°C for 3 minutes in the case of Fe. This step causes the catalyst to dewet and creates a bed of spherical catalysts that CNTs can grow from. Once the annealing phase is completed, the temperature quickly ramps to the growth settings simultaneously as a precursor gas, acetalyne (C_2H_2) [69], methane gas (CH_4) [70] or ethylane gas (C_2H_4) [71], can be introduced into the chamber. The growth temperature depends on the chosen precursor gas and is commonly set to 700 °C in the case of acetelyne. An illustration of the growth process is found in Figure 2.3. The growth time will directly control the height of the grown CNT arrays. The time/height relation is unique for every process chamber and is therefore a parameter that should be investigated carefully when tuning the process before material synthesis. The growth is finished by flushing the chamber with N_2-gas in order to terminate the process, which prevents the CNTs to grow further [72]. An illustration of the sample during growth can be found in Figure 2.4.

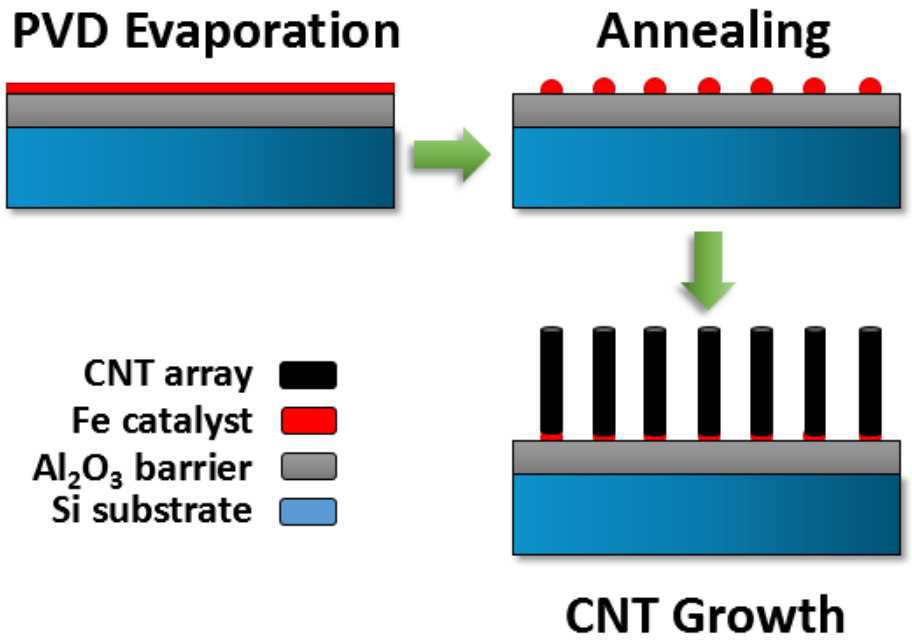


Figure 2.4: CNT growth substrate prepared using alumina and Fe as barrier and catalyst layers respectively. The figure depicts the different steps in the CVD growth process that includes catalyst annealing and CNT growth.

There are several ways to apply a CNT array as a TIM. The most common is the one-side interface, illustrated in Figure 2.5A, where the CNT array remains attached to the growth substrate and bonded at the CNT tips to another substrate. The one-sided configuration is a good choice if the growth substrate can be included into the final TIM [73–75]. Unfortunately, most CMOS applications are incompatible with the high processing temperature involved in the CNT synthesis which in turn restricts the use of one-side interfaces. A second type of interface is the transferred and double bonded interface, illustrated in Figure 2.5B. This is achieved by removing the growth substrate and attaching the CNT roots to another bond substrate [76–78]. This interface can circumvent CMOS incompatibility and would allow more applications where the TIM could be exploited [18]. This type of interface has the best potential for low thermal interface resistance performance, as some bonding techniques in literature are reported to reach lower thermal boundary resistances than what been measured at the catalyst/CNT boundary [79, 80]. Unfortunately, CNT array transfer will in most cases deform the array in the process which could impair the final TIM performance.

Alternative methods for bonding CNT arrays are the two sided interface and the interposer interface, illustrated in Figure 2.5C and 2.5D respectively. The two sided interface is achieved by pressing two CNT arrays against each other and thereby increase the low filling fraction of CNTs in the arrays. The main drawback here is that the CNTs no longer span the entire interface which should restrict heat transfer

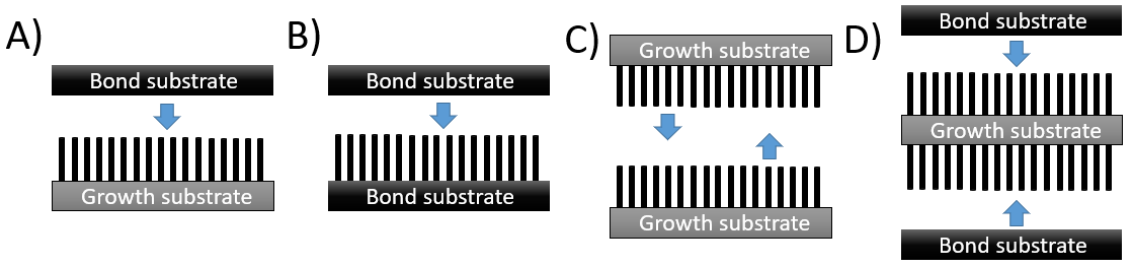


Figure 2.5: Different CNT array TIM configuration types. A) One-side interface. B) Transferred and double bonded interface. C) Two-sided interface. D) Interposer interface.

over the interface. This could be amended by fusing CNT strands together, which would enable direct connection of most CNT over the entire interface [81]. The last configuration covered is the interposer interface that can be used either as a thermal pad in dry contact or together with a proper bonding solution. The interposer type is achieved by growing arrays on both sides of a suitable substrate which in practice implies that this TIM can be used in any type of thermal package [82–84]. The resulting interposer would also be suitable for large BLT applications with the double arrays. However, this type of CNT array TIM would at the same time suffer from additional thermal boundaries that would increase the thermal interface resistance in relation to other CNT array TIMs.

The CNT array TIM design of choice can be fabricated once CNT arrays of desired height are synthesised. Depending on design, the bonding substrate needs to be adopted to the specific bonding solution of choice. Most TIM designs also require pressure and/or heating for bonding. By tuning pressure and temperature, a satisfactory amount of CNTs in the array will come in contact and bond with the mating substrate. However, this is a delicate process and slight misalignment during bonding will deform the CNT array and impair the resulting TIM performance.

2.2 Literature Review

The thermal resistance over the interface is inversely proportional to the amount of CNTs that are enabled to participate in the thermal conduction by directly bridging the interface. As CVD grown CNT arrays naturally exhibit a topology with a slight height difference, this can result in a considerable thermal boundary resistance. In order to solve this issue, three main bonding strategies are available as outlined in Figure 2.6. These are the dry contact, the metal based inorganic systems and polymer based organic systems. The difference between these strategies lies in how the CNT array tips are connected to the mating substrate. The same figure also outlines the different subcategories of the organic systems found in literature.

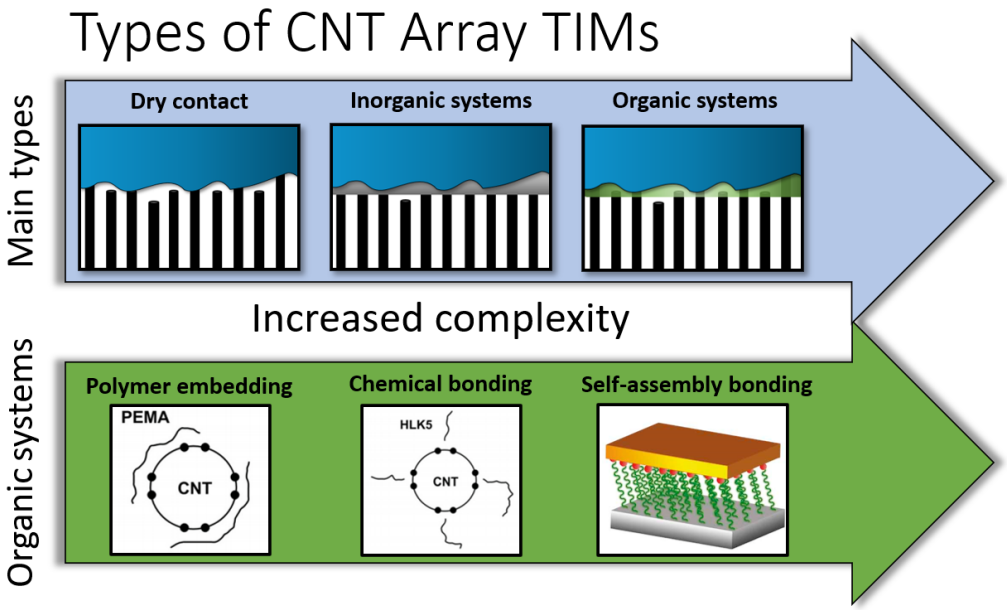


Figure 2.6: Different categories of CNT array TIMs found in literature. The top arrow represents the main types which includes: dry contact, inorganic systems and organic systems. The bottom arrow represents the subcategories within the organic systems category: polymer embedding, chemical bonding and self-assembly based bonding. Each of the arrows are ordered by system complexity from left to right. Adapted with permission from [85] and [86].

The dry contact type takes advantage of van der Waals forces in the contact interface between CNT ends and the mating substrate [87]. By applying a constant pressure over the interface, the array can conform to the substrate topology, thereby increasing the contact area which improves the van der Waals interactions in the interface [74, 88]. This type of CNT array TIM can be engineered by adjusting the surface roughness and by choosing an appropriate surface finish [75]. Several studies have measured the effective thermal interface resistance of dry contact CNT array TIMs using different contact substrates and have achieved thermal resistances of around 7 mm^2K/W [75].

Some researchers have experimented with bonding methods that embed the free ends of the CNT array in a metal coating on the mating substrate in order to improve the thermal boundary resistance [77]. This physical bonding locks the CNT ends in position under pressure and results in a CNT array TIM without the need of static pressure. The CNT array TIM can be engineered by varying the metallic coating thickness, which in turn will determine the required TIM closing pressure as well as how many of the CNTs in the array that will bond to the mating substrate. This will, in turn, determine the final performance of the CNT array TIM. To achieve a metal interface with low thermal boundary resistance, the metallic coating requires a low viscosity under reflow to allow CNT strands to efficiently penetrate the metal coating layer [72]. This method has been reported to achieve thermal interface resistance values down to 3.4 mm^2K/W [89] and as low as 1.7 mm^2K/W with additional static pressure [77].

Table 2.1: Summary of research related to organic functionalization methods for CNT array TIM. Here the BLT is given in µm and the R_{TIM} is given in mm^2K/W.

Description	**Bond material**	**BLT**	**R_{TIM}**	**Ref.**
Polymer embedding				
Si-CNT-PCM-Cu	PCM45F	10	5.2	[73]
Si-CNT-Wax-Ag	Paraffin wax	50	2	[92]
Si-Wax-CNT-Cu-CNT-Wax-Ag	Paraffin wax	50 (125)	10	[92]
Wax-CNT-Al-CNT-Wax	Paraffin wax	50	10	[93]
Si-CNT-Polymer-Cu	PEMA 300 nm	10	1.8	[94]
Si-CNT-Polymer-Cu	PEMA 600 nm	10	2.5	[85]
Si-CNT-Polymer-Ag	Polystyrene	10	8.5	[95]
Si-TCA-CNT-TCA-Cu	TCA	100	3.9	[96]
Si-CNT-Polymer-Cu	Polymer	10	5.7	[97]
Polymer bonding				
Si-CNT-Polymer-Cu	HLK5	10	1.4	[85]
Si-CNT-Polymer-Ag	P3HT	10	4.9	[95]
Si-CNT-Polymer-Cu	HLK5	10	9.5	[98]
Si-CNT-Polymer-Cu	HLK5	10	3.1	[97]
Self-assembly based bonding				
Si-CNT-SAM-Cu	Trimethoxysilane	100	10	[99]
Si-CNT-SAM-Al	APTES	70	0.6	[100]
Si-CNT-SAM-Au	Cysteamine	70	0.8	[100]
Si-CNT-SAM-Cu-Ag	Pyrenylpropyl	15	4.6	[101]
Si-CNT-nanoPd-Ag	nano-Pd	20	11	[81]
Si-CNT-nanoPd-CNT-Cu	nano-Pd	40	5	[81]

The thermal conductivity in all solid materials consists of both a vibrational (phonons) and an electron contribution. In CNTs, the phonon contribution to thermal conductivity dominates over the contribution of electrons [90]. Therefore, phonon - electron thermal mismatch in CNT/metal interfaces becomes a bottleneck for high performing metal interface based CNT array TIMs. By using a polymeric bonding agent instead, the contact resistance could in theory be decreased further than what is possible using the inorganic system approach. This is because a material with phonon modes that is compatible with the phonon carriers in CNTs could decrease scattering in the interface [91].

There are three directions in the field of organically bonded CNT array based TIM with different approaches. A summary of published results for organically bonded CNT array TIMs is listed in Table 2.1.

The most common approach is referred to as polymer embedding. This method uses a polymer of sufficiently low viscosity to penetrate into the array before curing, thus fixating the CNTs against the substrate. This method is similar to the metal bonding approach since no covalent bonds form between the CNT and the polymer. Phonon mode excitation matching is possible in the CNT-polymer interface, which allows improved phonon transmittance through the interface than in the case of CNT metal interface bonding [91].

The second discussed direction is the polymer bonding method. Like the organic embedding method the CNT arrays are also mechanically fixated inside a polymer phase to ensure an as high surface contact area as possible. Chemical bonding can also be exploited to decease the thermal interface resistance even further [102]. This can in principle couple the vibrational density of states (VDOS) of CNT with that of the functionalization molecule, as can be seen in Figure 2.7, to provide better phonon propagation through the interface.

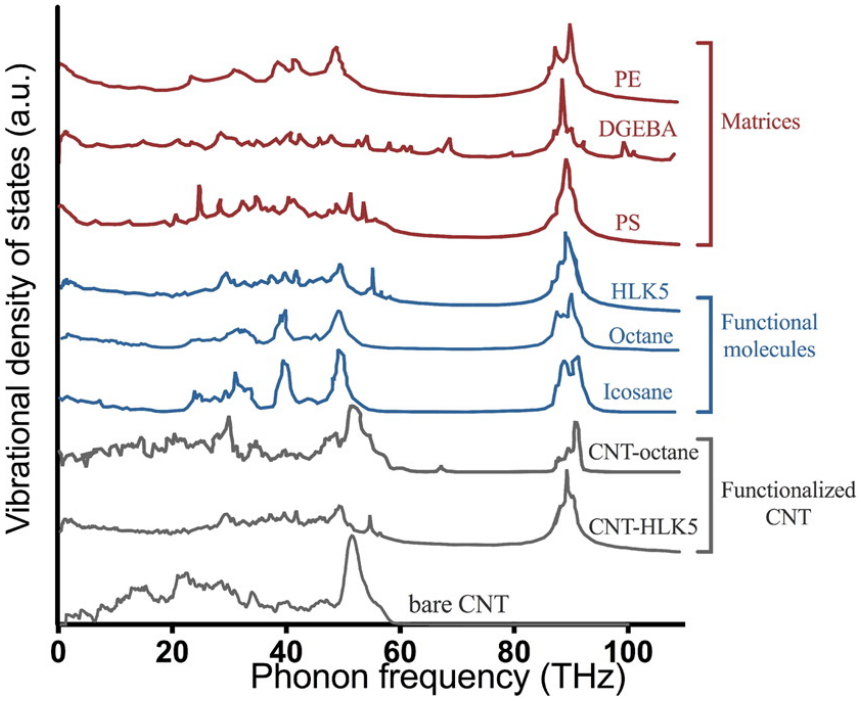


Figure 2.7: Comparison of the normalised vibrational density of states for different polymer matrices, functional molecules, functionalized CNT and bare CNT. Reprinted with permission from ref. [102].

In order to decrease the resistance even further in thermal packages, anchor points can be prepared using self-assembly based monolayers on the bond substrate. The third of the organic subcategories is therefore referred to as self-assembly based bonding. By using a monolayer of molecular anchors to bind and fixate the CNT to a substrate, a directed propagation of phonons can be achieved which could help phonons to transverse the interface [86]. As illustrated in Figure 2.8, molecular phonon couplers (MPCs) can self-assemble on the surface of a substrate before

bonding to the CNT array. This method allows the use of a atomically thin polymer layers that can minimize the thermal resistance in the interface and provide as direct phonon pathways as possible [103]. This is due to a decreased inelastic phonon scattering that otherwise would inhibit the TIM performance. The tails of the MPC can then react covalently with the CNTs or indirectly through π - π sidewall interactions that can absorb phononic modes. Some chemical functionalization methods will require defects in the CNT wall structure for covalent bonding to be possible which can be achieved by plasma etching. [86, 100]

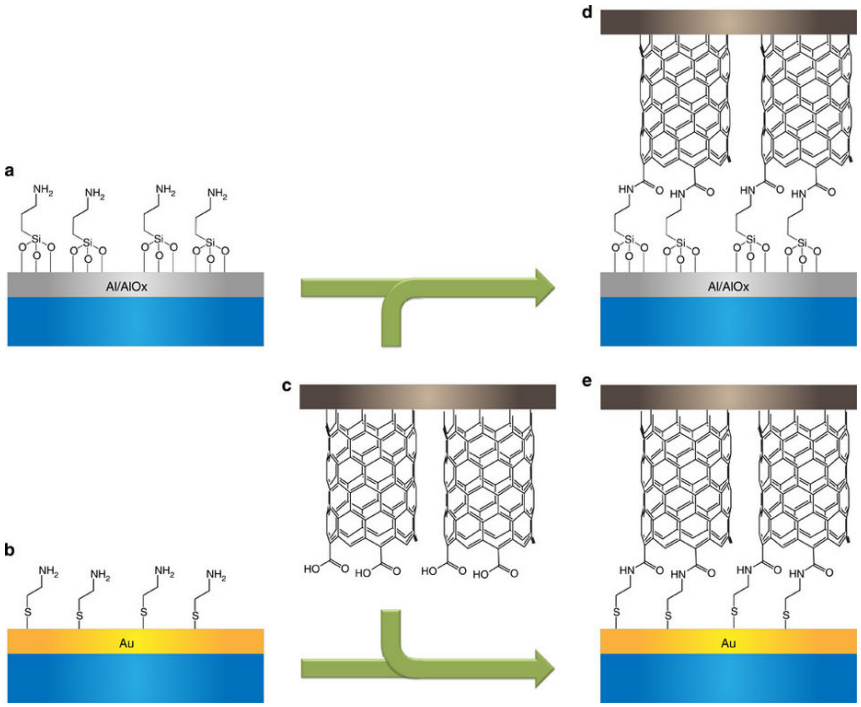


Figure 2.8: Self-assembled monolayers bond and bridge CNT arrays to substrates. Reprinted with permission from [100].

In summary, three different organic approaches to interface bonding of CNT array TIM have been discussed and the experimental results are summarised in Table 2.1. It is difficult to draw any relations between the height of CNTs and thermal resistance due to the low spread in array thickness and irregular results from the reported experiments. Like most TIMs, choice of interface solution is application dependent. Optimal performance will therefore be achieved by exploiting the advantages of different concepts to best suit the environmental demands for every product. By only comparing the best results from each of these methods it can be seen that the self-assembly based bonding approach could reach down to 0.6 mm^2K/W. This can be compared to bonding and embedding type interfaces with thermal resistances that results in about two and three times higher resistance values respectively. Additionally, further improvements to these numbers should be possible when comparing results from corresponding metal bonding techniques as polymers can allow better matching of CNT phonon VDOS.

Even though many of the findings in literature match and surpass the traditional PLP and solder based TIMs, no commercial products can be found yet based on CNT array structures. This has most certainly to do with the lack of large-scale fabrication methods that can ensure high quality CNTs. Furthermore, none of the surveyed articles include reliability studies with proper cycling and failure analysis. The reliability is an important aspect to take into account if CNT array TIMs are expected to reach commercial success in the future.

2.3 Design, Fabrication and Evaluation of CNT array TIMs

2.3.1 Self-Assembled Monolayer

It is important to understand the thermal transport mechanism in CNT array TIMs to successfully decrease the thermal boundary resistance. By bonding the CNT using a metal that utilises electrons as thermal carrier, the phonon energy needs to be converted at the interface to an electron carrier. This phonon - electron mismatch therefore acts as a limiting factor in all metal-bonded CNT based TIMs [91]. Organic functionalization materials in which the thermal transport is also phononic in nature, should thus be explored to couple vibrational states between the polymer and CNTs. In order to exploit this behaviour, covalent coupling is required between the CNT and mating substrate to allow optimal phonon transport over the interface. However, bonding the CNTs in a polymer layer would, in principle, result in a dampening effect that could reduce the phononic transport over the interface. This effect has been demonstrated with poly(ethyl methacrylate) (PEMA) functionalization [85, 94]. Reducing the bond layer from 600 to 300 nm thickness resulted in a 28% improvement in terms of thermal interface resistance. Taking this principle further, the perfect organic functionalization would only consist of one molecule thick layer which contacts all of the CNT tips covalently to the mating substrate. One such solution is using self-assembled monolayers with appropriate head groups that can covalently anchor the CNT tips at the surface [100]. This chapter is based on Paper B, which deals with the fabrication of epoxy-silane based monolayer CNT array TIMs.

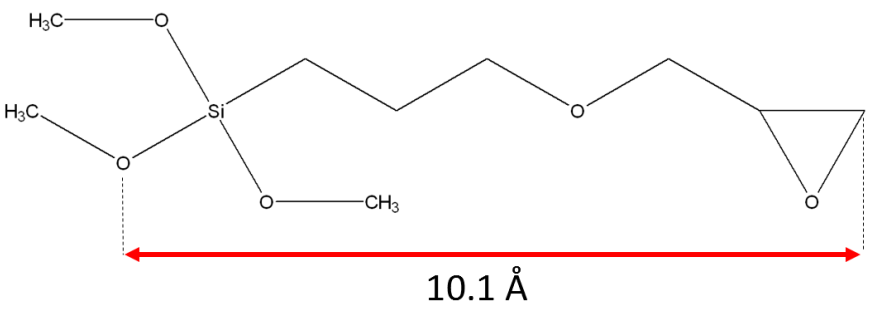


Figure 2.9: Epoxy silane molecule used as covalent coupler for CNT array TIM.

Monolayers of epoxy silane ((3-Glycidyloxypropyl)-trimethoxysilane (GLYMO), illustrated in Figure 2.9) was explored for use as covalent anchoring medium in CNT array TIMs. This molecule has a trimethoxysilane backbone for the self-assembly together with an epoxide group that is intended for covalent bonding with CNTs. Epoxides can form covalent bonds together with a range of different functional groups, like nitrogen containing amines. Therefore the CNTs can use nitrogen modification that creates these functional groups on the side walls to facilitate successful bonding to the epoxy silane monolayer [104].

The intended CNT array TIM is composed of two main parts: the epoxy silane functionalized Si bond substrates and the CNT array covered Si growth substrates, both of which are illustrated in Figure 2.10.

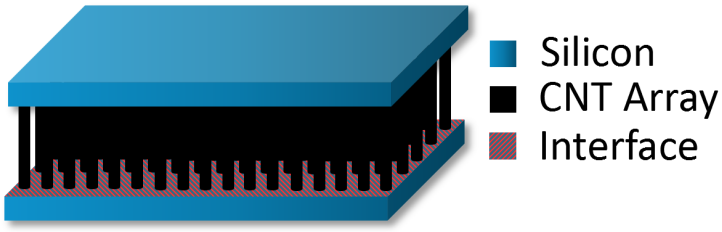


Figure 2.10: Typical one-sided interface CNT array TIM assembly composed of two Si substrates bonded together by a CNT array fixated by a GLYMO coating.

Silicon substrates with a 12 nm thick native oxide were used for the epoxy silane functionalization. The substrates were cleaned from any organic contamination and subsequently protonated in a 3:1 piranha etching solution [105]. A functionalization bath consisting of 80 vol% cyclopentanone, 10 vol% methanol and 10 vol% (3-Glycidyloxypropyl)-trimethoxysilane (epoxy silane) was used to functionalize the silicon substrates [106]. After silane coating, the silane - silicon oxide reaction was quenched by rinsing the substrates in pure methanol and de-ionized water (DI). The silane functionalized substrates were stored in DI-water over night to render the silane monolayers hydrolytically stable [107]. This process is found in Figure 2.11.

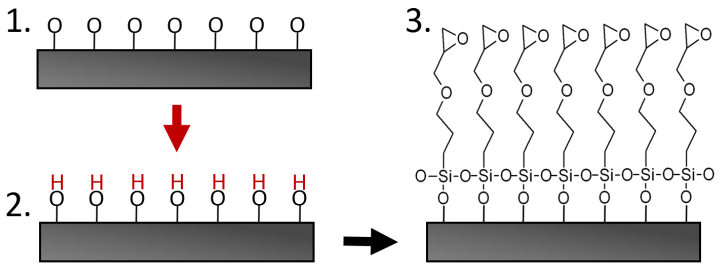


Figure 2.11: Silane functionalization process. 1: A uniform thermal oxide is grown on silicon substrates. 2: Protonation of the oxygen sites on the wafer is achieved by submersion in piranha solution. 3: The -OH groups can now react and bond to the silane molecules.

The quality of the as-prepared epoxy silane substrates was analysed in terms of surface coverage and composition using ellipsometry, atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS) techniques. An ellipsometric height map of the samples is shown in Figure 2.12. The surface of a silicon substrate was measured before silane deposition and the average thickness of the oxide layer was used in the model to describe the layers underneath the silane monolayer. After monolayer deposition, the average measured thickness of the top layer was found to be 0.95 nm over the entire region. These values are therefore in agreement with the expected thickness of the 1 nm of a bonded epoxy silane monolayer, as can be seen in Figure 2.9.

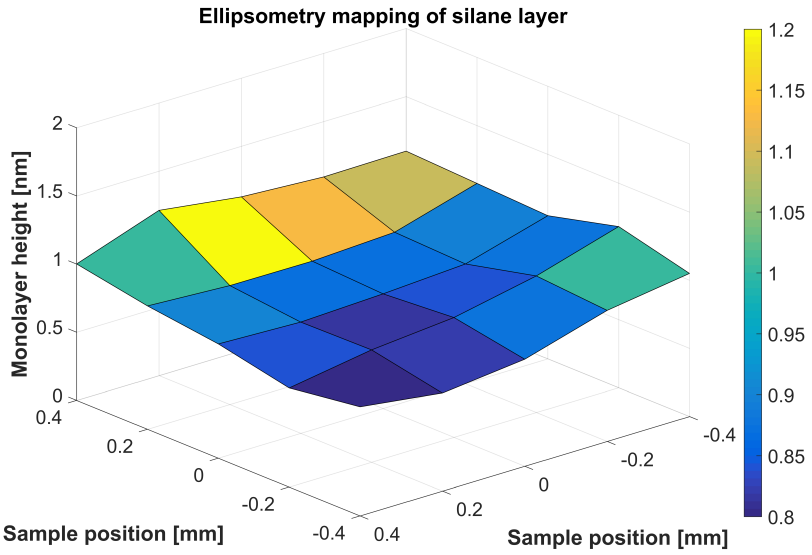


Figure 2.12: Mapping of the epoxy silane thickness across a silicon substrate surface obtained by ellipsometry.

It is important to avoid island growth for the silane layer since this will actively decrease the area where covalent bonding with CNT can take place. By using AFM as a compliment to the ellipsomitry data, a more detailed height mapping of the surface could be obtained and analysed for the samples. Figure 2.13A shows a sample with bad surface coverage in comparison to a sample with full coverage that can be seen in Figure 2.13B. A complete coverage of the surface is characterised by having a low surface roughness in comparison to the theoretical monolayer thickness. The measurement from Figure 2.13B gives a surface roughness of 0.16 nm that can be compared with the 0.25 nm roughness of the silicon substrate that was measured before silane coverage. This decrease in surface roughness after monolayer coating has been observed previously for similar silane based monolayers on silicon substrates [108].

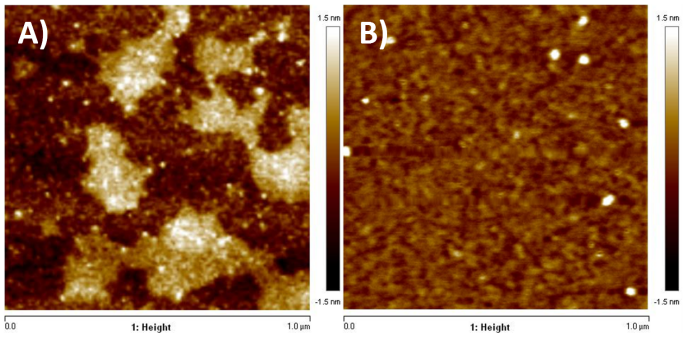


Figure 2.13: Typical AFM measurement on the functionalized Si substrates: A) silane islands, B) complete silane coverage.

Elemental characterisation of the silane substrates was carried out using XPS. As seen in Figure 2.9, the main bonds present in the epoxy silane molecule are the epoxy group at 286.1 - 287.1 eV, -C-O-C- ether found between 286.1 - 288.0 eV and the sp^2 bonded carbon around 284.3 - 284.6 eV [109]. An XPS spectrum of the carbon peak obtained from the epoxy silane modified substrate can be seen in Figure 2.14. Three components could be identified through deconvolution: Peak #1 at 287.5 eV, peak #2 at 286.1 eV and Peak #3 at 284.5 eV. These peaks can be matched with the different parts of the epoxy silane molecule where Peak #1, #2 and #3 correspond to ether, epoxy and sp^2 components respectively. It is worth mentioning that the organometallic silane component found in the epoxy silane molecule is stated in literature to appear at 284.4 eV, which means that it disappears in the sp^2 peak [110]. This also implies that the intensity of Peak #3 is elevated in relation to the other peaks present.

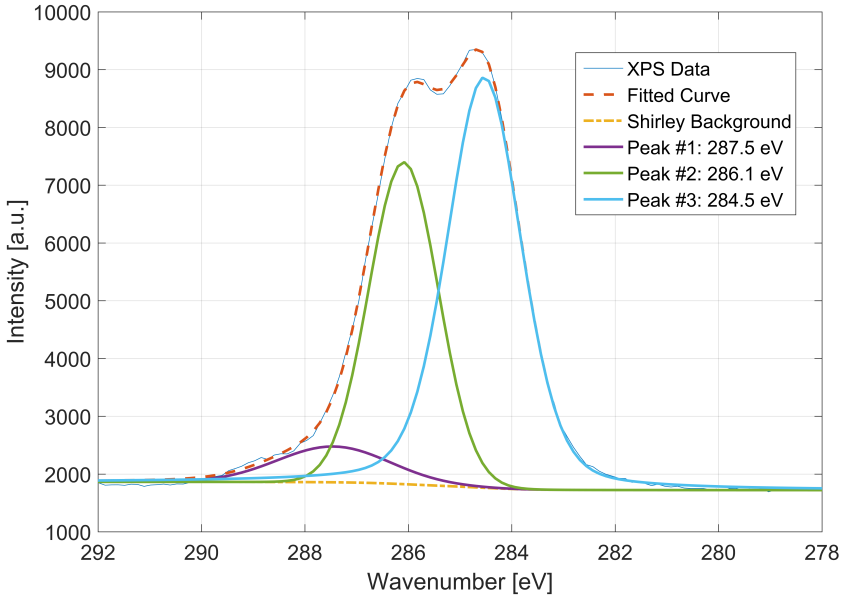


Figure 2.14: Deconvolution of C1s part of the XPS spectrum from the epoxy silane modified Si substrates. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

The topological and elemental data acquired from the modified substrates shows that homogeneous monolayers of epoxy silane molecules were successfully formed on the surface of the Si substrates.

Amino groups were embedded into the CNT wall structure of the arrays intended for the interfaces to provide the CNTs with the necessary chemical functionality for covalent bonding to occur with the epoxide groups found on the silane monolayer. This was achieved by exposing the CNT arrays to plasma using a 2:1 volume mixture of nitrogen and hydrogen gas. The CNT samples after plasma treatment were measured using XPS multiplex scans. To find the nature of the infused species after treatment, the C1s and N1s data were peak fitted to their individual contributions.

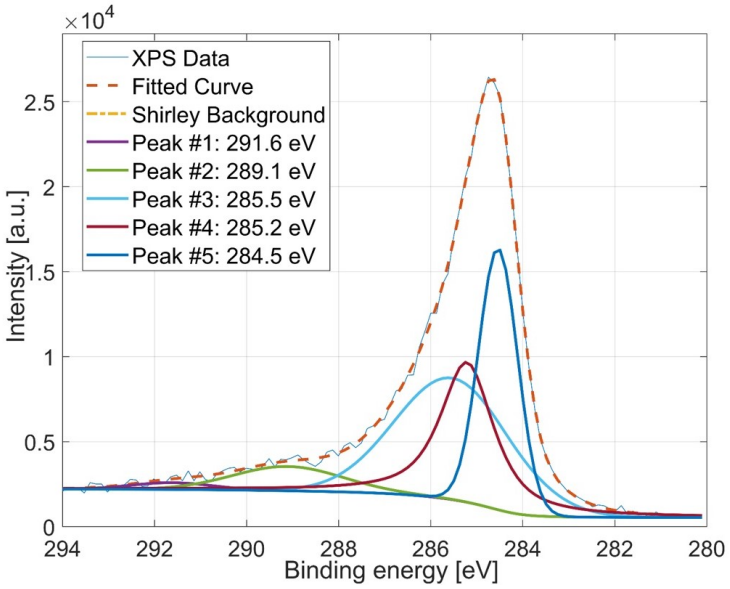


Figure 2.15: Deconvolution of C1s part of the XPS spectrum from the nitrogen plasma modified CNT arrays. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

The peak fitting results of the C1s data can be found in Figure 2.15. Here, three main and two minor components could be extracted. The main peaks (Peak #3-5) are located at 285.5, 285.2 and 284.5 eV and the minor peaks (Peak #1 and #2) at 291.6 and 289.1, respectively. By comparison, the location of these peaks in the spectrum could be matched with reference data and corresponding functional groups could be identified [109]. Peak #5 correspond to the sp^2 bonded carbon which is the main lattice of the CNT structure. Peak #4 was found to be an sp^3 peak which originates from amorphous carbon as well as eventual damages to the CNT structure after plasma etching. An amino peak could also be matched to peak #3; this is an indication that the plasma treatment successfully created amino functional groups embedded into the CNT structure. Two minor peaks, peak #1 and #2, are matched with smaller amounts of fluorine carbon and oxygen containing compounds that might have appeared during the sample processing.

The N1s data from Figure 2.16 was also fitted in order to gain more information about the nitrogen present in the CNTs. Two peaks could be extracted; Peak #1 at 400.4 eV and Peak #2 at 398.8 eV. It has been reported that pyridine and nitrile in CNT specimens can give rise to peaks around 398.5 and 398.8 eV [111]. Other nitrogen containing groups like amine and amide have in literature been found at binding energies ranging from 399.5 - 400.5 eV [112].

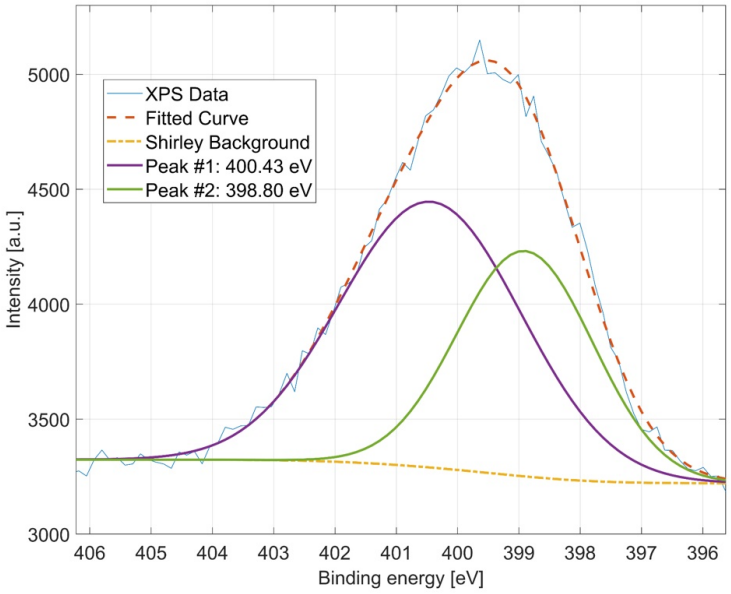


Figure 2.16: Deconvolution of XPS spectrum acquired from the N1s spectrum acquired from the nitrogen plasma modified CNT arrays. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

With the information obtained from Figure 2.15 and 2.16 we can draw the conclusion that the CNT tips were successfully activated with amino functional groups using nitrogen plasma. The plasma treatment resulted most prominently in amino groups together with smaller amounts of pyridine and/or nitrile on the surface of the CNT array. Additionally, small trace amounts of fluorine and oxygen bounded to the CNT structure could be detected which was judged not to affect the process in any significant way.

The closing of the interface between the silane functionalized silicon substrate and the amino activated CNT array was made using a custom-made clamp. The parts were pressed together in a oven under nitrogen atmosphere to facilitate chemical epoxy bonding of the CNTs to the mating substrate.

The thermal interface resistance of the fabricated samples were measured using the laser flash technique. The thermal interface resistance could be extracted by treating the CNT array as a contact resistance in-between the two substrates. This is done using an approach called two layer plus contact resistance method and requires knowledge about the properties of the surrounding substrates before the $R_t h$ can be extracted [113]. A cross section of the CNT based TIM is illustrated in Figure 2.17 together with a thermal resistance circuit that explains the thermal resistance contributions taken into account in these measurements. By disregarding the thermal bulk resistance of the two silicon substrates we can separate the two contact resistances R_{C1} (CNT catalyst side) and R_{C2} (coating side) and the thermal bulk resistance of the CNT array denoted ΣR_{CNT} (according to Equation 1.3).

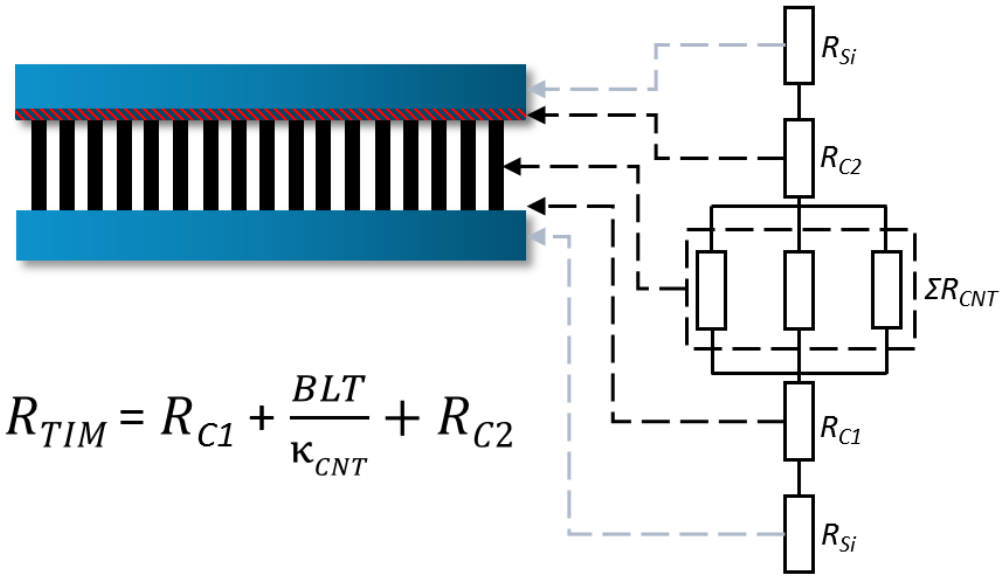


Figure 2.17: Cross section of the CNT array TIM together with a thermal circuit. The thermal resistance values obtained for these TIMs are the sum of the two thermal contact resistances on either side of the CNT array together with the bulk thermal resistance of the CNT array.

Results from the experiments on the GLYMO bonded CNT array TIM design were compared to reference samples which showed a thermal interface resistance of 47 mm^2K/W and around 5 % improvement to reference. These results are presented in Figure 2.18. This means that this design still requires some work before it can compete with other CNT array TIM solutions from literature. However, the improvement compared to reference samples shows that signs of a slight effect of the GLYMO functionalization. This design will require further studies on the amino functionalization and the closing procedure to confirm that the epoxy reaction will work the way its intended to.

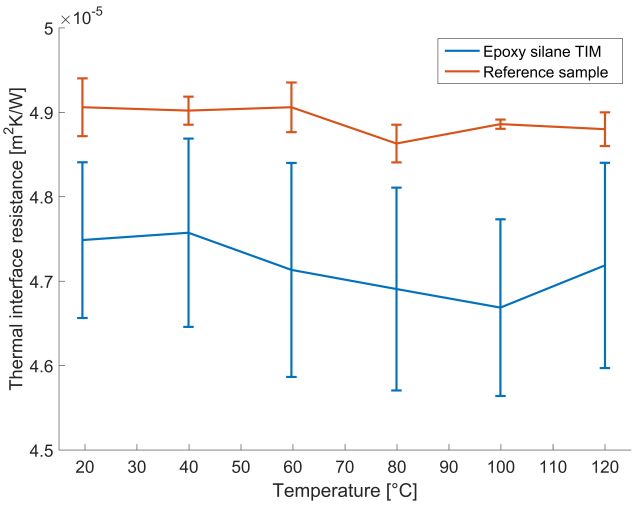


Figure 2.18: Averaged thermal measurement results for three of the CNT array TIMs bonded with the epoxy silane MPCs plotted against a reference sample. Here the error bar represents the standard deviation of the results for all the measured samples.

2.3.2 Polymer Bonding Through Azide Chemistry

One of the research projects I was involved in during my Ph.D. study was aiming to scale up production of HLK5 functionalized CNT array TIMs to industrial volumes [102]. This solution was coincidentally found to be the most promising to date from the literature study found in Paper A. Several papers are published on the technology concerning topics raging from molecular dymanics simulations (MDS) [102] to experiments regarding production methods [97, 98, 114]. According to published data, this solution can reach a thermal interface resistance as low as 1.4 W/mm^{2}K [85]. As the new interfaces would be fabricated using components from new suppliers it was of importance to confirm that the final interface could match the previously reported results. Therefore, a characterization study of the new interfaces was performed and those results were published as part of Paper C.

The HLK5 molecule is a co-block polymer with azide and benzene functional groups illustrated in Figure 2.19. This molecule can graft into the CNT lattice with the azide group and form a strong C-N anchoring of the CNT array to a substrate. As the polymer forms long chains and at the same time possesses a low glass transition temperature, T_g, the CNT tips will be able to penetrate and embed themselves within the polymer coating which provides a good connection for thermal transport [85]. Though MDS it was found that the benzene groups would allow further thermal transfer by $\pi - \pi$ stacking interactions that allows a matching of VDOS modes [102]. Experimentally, HLK5 was shown to reduce the thermal interface resistance by more than 40 % when comparing to PEMA, a polymer that provides a similar embedding but without the covalent anchoring.

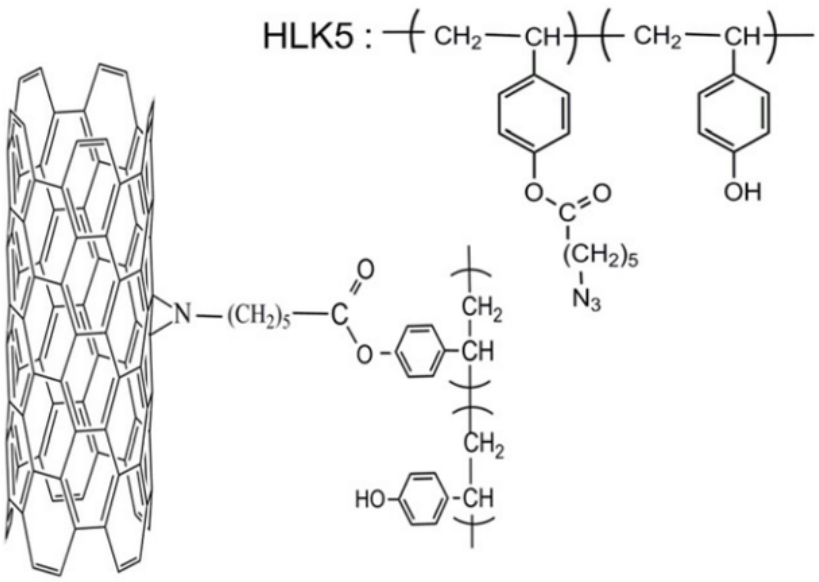


Figure 2.19: Molecular representation of the HLK5 polymer that is used to bond to the CNT lattice in CNT array TIMs. Adapted with permission from [85].

In our study the interfaces were fabricated using a Si substrate with a 15 µm grown CNT array bonded to a Cu heatsink with a spin coated HLK5 polymer. The interfaces were closed using a autoclave process in order to apply an even pressure over the interface. The resulting interface is illustrated in Figure 2.20.

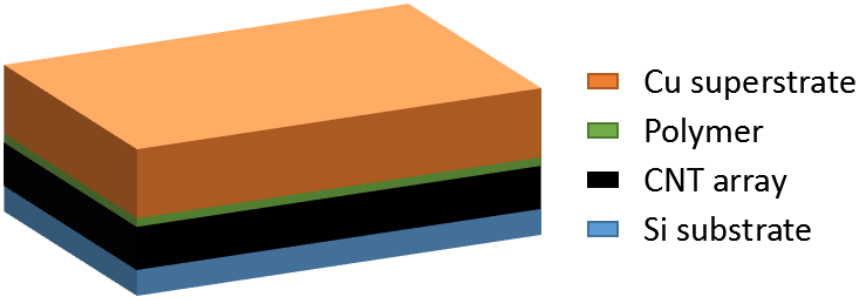


Figure 2.20: Cross section of the CNT array TIM fabricated using the HLK5 polymer.

Two measurement methods were used to eveluate the thermal resistance contributions in the CNT array TIM system: laser flash and pulsed photothermal reflectance (PPR) [115]. The impact of the HLK5 functionalization could be calculated by finding the thermal bulk conductivity of a free-standing CNT array and the thermal interface resistance at the CNT/Si interface and comparing to the total interface resistance.

Identical CNT arrays to the ones used in the CNT based TIM samples were investigated using a PPR setup in order to find the effective thermal conductivity κ_{CNT} as well as the thermal interface resistance between the CNT array and the silicon substrate R_{C1}. As the CNT arrays used to fabricate the investigated TIMs

originated from the same batch, the quality (κ_{CNT} and R_{C1}) was assumed to be identical. Thermal properties could be extracted after fitting parameters to the signal accordingly and an effective thermal conductivity, κ_{CNT}, of 71 W/mK and a thermal boundary resistance, R_{C1}, of 0.96 mm^{2}K/W was found.

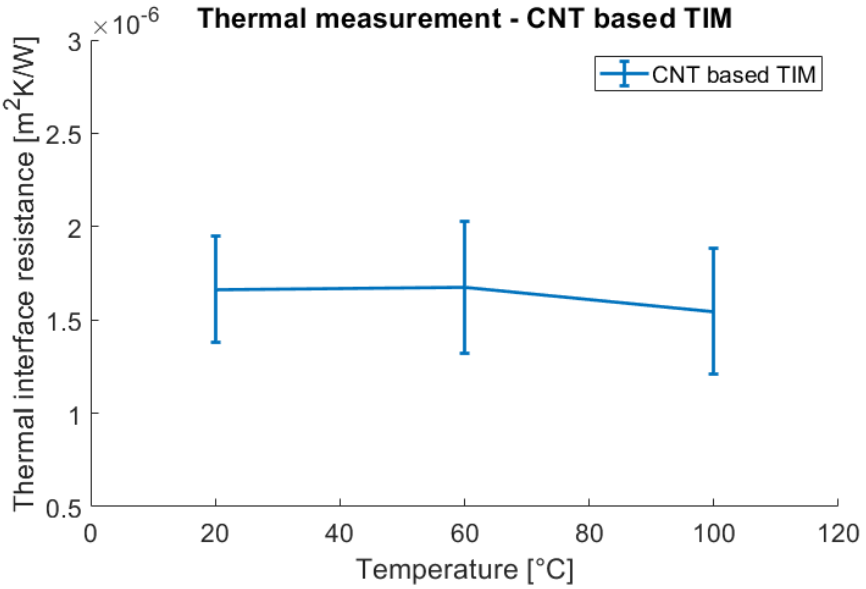


Figure 2.21: Results from the initial laser flash measurement of the CNT based TIM.

With the R_{TIM} value obtained from Figure 2.21 together with the κ_{CNT} and R_{C1} result from the PPR measurements, R_{C2} can be calculated using the thermal interface relation stated in Equation 1.3. This relation gives a R_{C2} of 0.49 mm^{2}K/W for the CNT based TIMs. By comparison, this means that the polymer functionalization is about twice as good as the CNT-Si boundary on the other side of the interface in terms of thermal boundary resistance. This calculation assumes 100 % of the array tips in contact with the polymer coating on the mating substrate which might seem optimistic. However, this assumption should be quite close to the truth according to the comparably low thermal interface resistance measured over the interface. This result further confirms the importance of using a bonding medium that allows proper penetration by the CNT tips. This was made possible in this case due to the low T_g of HLK5.

2.3.3 Carbon Nanotube/Graphite Thermal Interposer via Joule Self-Heating

To utilize CNT arrays for second level TIM (TIM2) applications there is a need to grow the materials to fit the BLT requirement between the IHS and heatsink [116]. Thermal pads used for TIM2 applications are designed for easy deployment, re-usability and often comes with a thickness of at least 1 mm [117]. Carbon nanotubes

however are difficult to grow longer than 700 - 800 µm without using special methods [118, 119] and comes with CMOS compatibility issues. One way to circumvent these issues is by designing the TIM as an interposer structure. Growing CNT arrays on both sides of a substrate enables standard growth methods to reach thicker dimensions up to and beyond 1 mm and makes it easy to deploy the TIM in systems that otherwise would be practically difficult.

While depositing catalyst on both sides of a film is easy in itself, issues arise during growth. Hot wall CVD is traditionally used when there are strict requirements on temperature control. However, this method is also time consuming and the power consumption is much grater than that of cold wall CVD systems. Instead of heating the entire reactor, cold wall CVD systems relies on a localized heater. The heater is often made of graphite and used to heat a sample using the joule heating effect. To be more specific, it is the catalyst particles that are required to reach the growth window and therefore extensive system tuning is required to ensure the correct heater temperature so desired sample quality can be reached. Unfortunately, this implies that a double sided growth would remove the catalyst particles further and further away from the heater as the growth progresses when the CNT array on the backside of the interposer grows. This would result in a sample with a gradual decrease of CNT growth quality which would result in a self-termination once the growth substrate is too far away from the heater. A solution to this issue was found by rethinking the heater design all-together in the cold wall system used for CNT synthesis. This was done by modifying the existing cold wall system and changing the graphite heater to a graphene-based film [120], which can act both as growth substrate and joule heater simultaneously. This way, a uniform heating of the catalyst particles was achieved and a continuous growth quality could be ensured throughout the process even for longer array heights. Illustration of an ordinary CVD setup and the modified reactor is illustrated in Figure 2.22.

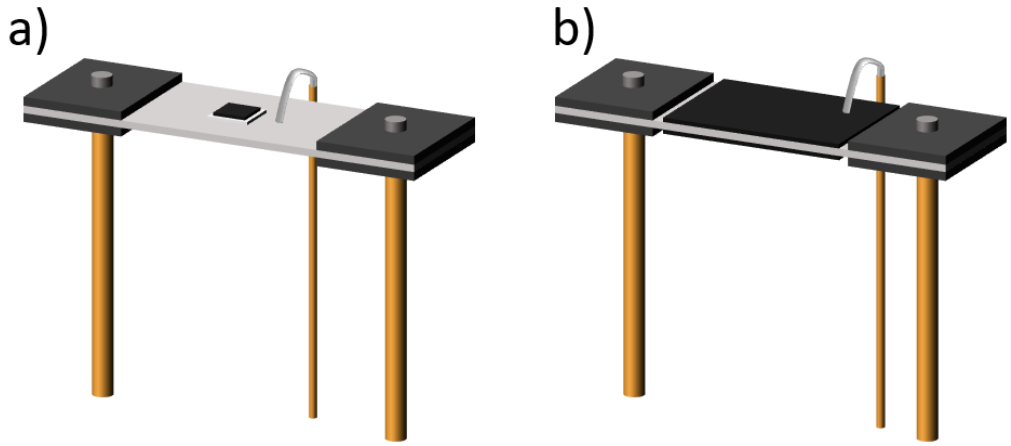


Figure 2.22: a) Ordinary CVD growth of CNTs where a chip is placed on the graphite heater and b) Modified version of the CVD reactor which uses the growth substrate as heater.

A graphene film was used for the interposer growth that prior to experiments was heat treated at 2850°C in order to improve the thermal properties of the film. Therefore, the film has been reported to possess an in-plane thermal conductivity that is 60 % higher than that of commercial pyrolytic graphite sheets (PGS) that the standard graphite heater is made of [120]. This film was not as rigid as standard PGS tend to be and some trial and error was required to find correct settings in terms of tension of the film and positioning of the thermocouple before the desired growth results could be achieved. As the joule effect is dependent on the electrical and thermal properties of the heater, this film performed well and the growth only consumed about 25% compared to the normal heater in order to reach the growth window. However, the joule effect heating results in a lower temperature around the edges. Therefore, materials grown using this method should be expected to exhibit shorter growth on the edges of the film [121–123]. The edge effect can be seen in Figure 2.23a where the color between the gray graphene film on the side and the CNT array black in the middle section indicates poor growth. This issue was circumvented by patterning the film prior to catalyst deposition as seen in Figure 2.23b.

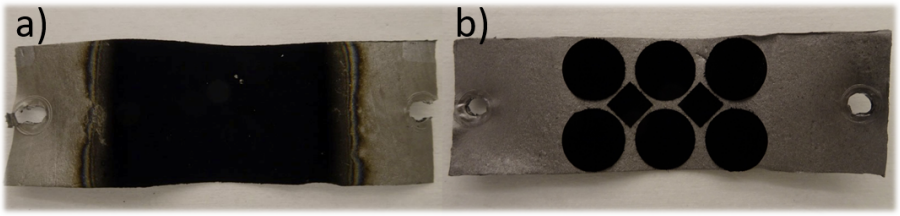


Figure 2.23: a) Unpatterned graphene CNT hybrid film and b) film with patterning.

The CNT length is not the only factor to take into account when assessing the overall growth quality. Strand uniformity and crystallinity are also factors that will determine the thermal, electrical and mechanical properties of the CNT [68, 124]. Scanning electron microscopy (SEM) images of the final sample is presented in Figure 2.24 with both a side view of the entire interposer as well as a magnification of the CNTs themselves, both of which indicate satisfactory results in terms of array length and alignment.

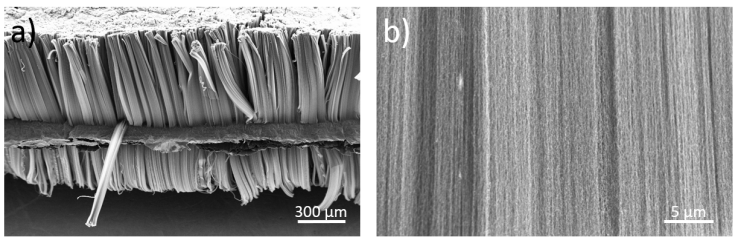


Figure 2.24: SEM image of a) side view of the graphene CNT hybrid interposer TIM, b) magnified view of the uniform growth of CNTs this method can produce.

Many of the properties sought after in CNT materials are affected by the crystallinity. Thermal, electrical and mechanical properties can be improved significantly with higher crystallinity [125, 126]. For a second level interposer style TIM, thermal conductivity is important and therefore it is of interest to evaluate how good quality CNTs it is possible to grow using this method. This was evaluated using Raman spectroscopy and the results are presented in Figure 2.25.

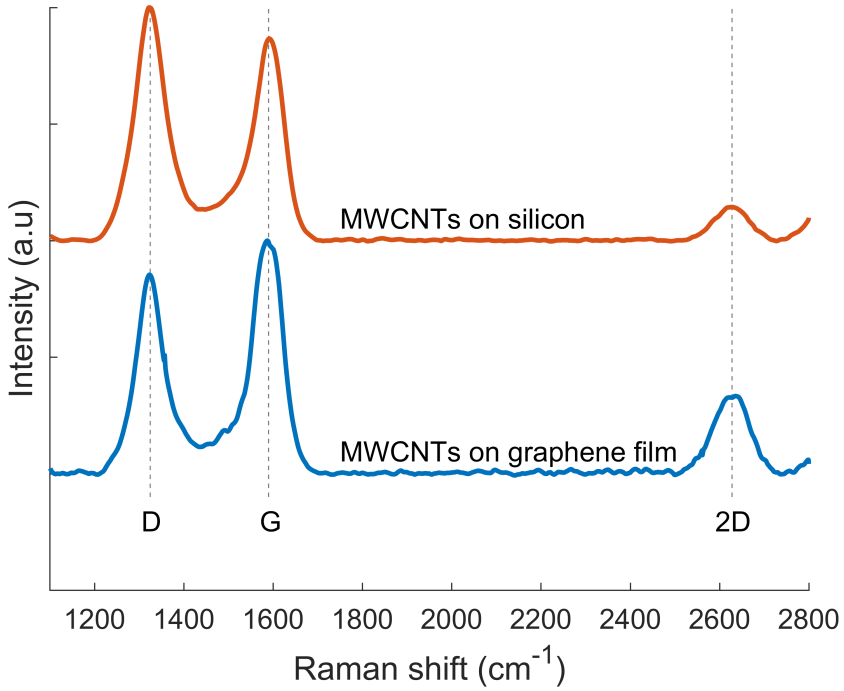


Figure 2.25: Raman spectrum of a standard CNT grown on Si substrate compared to the CNT grown on the graphene film.

A comparison of the D/G ratio from Figure 2.25 of the CNTs on the graphene CNT hybrid film to reference CNTs indicates that the crystalinity of CNTs on the hybrid film indeed is higher. This would indicate that the growth of CNTs using this novel method produces as good or even better CNTs than the standard method that uses Si chips. This is somewhat unexpected since CNT growth on Si is a mature process that has received extensive academic attention [127]. The root cause of this increased crystallinity might originate either from a better compatibility of the graphitic substrate with the CNTs, or more likely, an improved temperature control that is possible from the direct heating that the modified CVD process offers. As the hybrid film is intended for thermal management applications, thermal conductivity is the most important metric of the CNT quality. This was assessed using the PPR method as well as the TIM test method based on the ASTM D5470 standard [128]. The results from these measurements are presented in Figure 2.26.

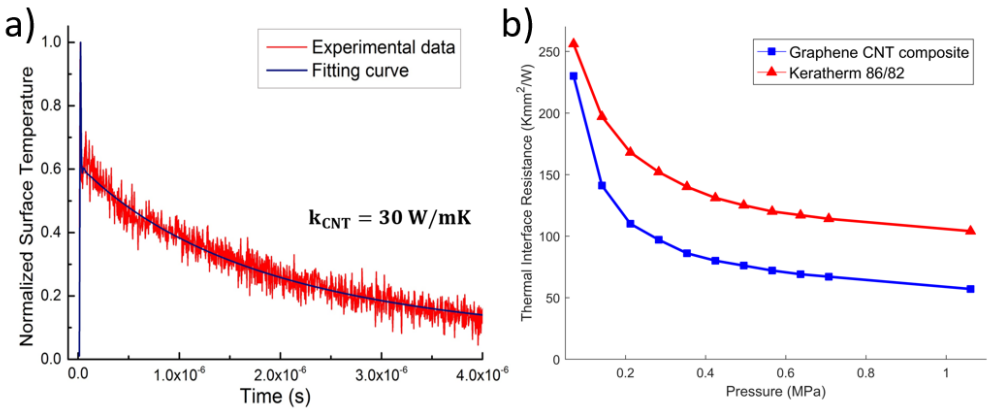


Figure 2.26: Results from the thermal measurements of the graphene CNT hybrid film: a) PPR measurement of the CNTs on the film and b) effective thermal resistance measurement of the whole interposer using ASTM D5470 TIM test.

The thermal conductivity of CNTs grown on the graphene film was evaluated and measured to be 30 W/mK. This is lower than half of the thermal conductivity measured on the CNTs on Si substrates using the same PPR method discussed in Chapter 2.3.3. Once again, this result is somewhat surprising as the improved crystallinity should result in a higher thermal conductivity of individual CNT strands. However, the graphene-based film will also play a role and could theoretically result in a lower density growth of CNTs due to affected of surface potential of the Al_2O_3 under-layer compared to growth on normal Si growth substrates [129]. If so, higher thermal conductivity should be attainable through a careful tuning of the catalyst under-layers. This matter does however require more attention in order to draw definite conclusions.

Through-plane conductivity of the graphene film also has an impact on the total thermal resistance of this TIM and has previously been determined to be 15 W/mK [120]. In this case, the graphene-based film was compressed down to 10 µm thick sheets before growth which gives a resistance of 0.67 mm^2K/W.

Simulated TIM performance was evaluated using the ASTM D5470 TIM test to find the total effective thermal resistance of the graphene CNT hybrid film. Thermal pads require at least 0.7 MPa of pressure in order to achieve optimal performance [130]. Therefore, the same test principle was used for the graphene CNT hybrid film. The thermal resistance results of the graphene CNT hybrid film compared to a commercial high performance thermal pad (Keratherm 86/82 [131]) used as reference can be found in Figure 2.26b. The results show that the graphene CNT hybrid film delivers a resistance of 68 mm^2K/W at 0.7 MPa, compared to the reference thermal pad that offers 115 mm^2K/W which is about 70 % higher resistivity at the same pressure. The total thermal resistance of the graphene CNT hybrid can be expressed as equivalent to an electrical circuit as following:

$$R_{TIM} = R_C + \frac{BLT_{CNT}}{\kappa_{CNT}} + R_{CNT/GF} + \frac{BLT_{GF}}{\kappa_{GF}} + R_{CNT/GF} + \frac{BLT_{CNT}}{\kappa_{CNT}} + R_C \quad (2.1)$$

The thermal resistance equivalent circuit of this kind of double sided CNT array interposer will have 4 contact resistances, 2 bulk CNT contributions and 1 contribution from the through plane thermal conductivity of the graphene film. Some conclusions can be drawn by calculating the known values regarding the bulk thermal resistance of the system through Equation 2.1. The measured values for the CNT arrays (500 µm and 30 W/mK) give a thermal resistance of 16.7 mm^2K/W per side and the resistance contribution for the graphene film is 0.67 mm^2K/W, which gives a bulk resistance of the interposer that is equal to 34 mm^2K/W. That means that the remaining 34 mm^2K/W originates from the connection points of the CNT arrays to the graphene film, $R_{CNT/GF}$ as well as the contact resistances on either side of the ASTM D5470 measuring device R_C. The interface resistance of CNT arrays to Si growth substrates was previously measured in Chapter 2.3.2 in the order of a single mm^2K/W. Therefore, it is probable that this sample will possess a contact resistance between the CNTs and the graphene film of the same order of magnitude too. Previous work on dry contact based CNT array TIMs has shown thermal interface resistance values of around 7 - 15 mm^2K/W which would explain the remaining contact resistance [75, 92, 132].

The joule self-heating fabrication of graphene CNT hybrid TIMs has demonstrated promising results from these initial trials. Characterization of the CNT array revealed a slightly lower concentration of defects together with a unusually low thermal conductivity compared to CNT arrays grown on standard Si growth substrates. The fabrication method was determined as a probable cause for the lower amount of defects due to the higher degree of heating control that is possible. At the same time, the low thermal conductivity might have to do with a low CNT array density. Further studies should therefore focus on improving the array density and tuning the CNT length without sacrificing reliability. By combining this interposer structure with suitable bonding solutions like the HLK5 coating, substantial thermal interface resistance improvements will be possible.

2.4 Summary and Conclusion

Improvement of thermal management performance and reliability is in high demand as the industry continuously increases the TDP ratings for IC devices every consecutive year. For this purpose, CNT array TIMs have potential to fill the void between current commercially available TIMs that either delivers high performance or are proven for reliability.

This chapter has introduced the field of thermal interface materials based on carbon nanotube arrays. Subjects from synthesis, design perspectives and a review of the field have been covered. The chapter also presents my own work on three different types of TIM solutions based on carbon nanotubes: A novel TIM1 bonding method utilizing self-assembly based anchoring through epoxy chemistry, measurements on an HLK5 functionalized TIM1 solution as well as a novel graphene CNT hybrid interposer structure for TIM2 applications.

Even though many of the results on CNT array TIMs seem promising in literature, the full potential lies in combining the high thermal conductivity of the CNTs with engineered interfaces that removes possible thermal constrictions. One identified bottleneck is the contact resistance between CNT and growth substrate through the catalyst under-layers which results in a comparably large thermal contact resistance. By focusing on transfer methods for double side bonded interfaces, this bottleneck can be removed and will make the technology more versatile for applications.

Chapter 3

Reliability Investigation of Carbon Nanotube array Thermal Interface Materials

CNT array TIMs have been demonstrated by several research groups to show potential to replace current commercially available TIM solutions [73, 92, 133]. However, such a solution needs to be proven for reliability and quality before the technology would be regarded as mature enough for an industry adoption.

The mechanical properties of a CNT array TIM are different from ordinary TIM solutions like solder and grease due to the nanowire forest structure that connects two substrates together over an interface. This is due to the mechanical buffer that should form during bonding as the array is compressed and the CNTs are curled together inside the array. The potential of this buffer becomes even larger due to the flexibility of CNTs themselves [134] and due to the mechanical decoupling of the array in the horizontal plane of the interface. All of these factors should allow the CNTs to absorb stress originating from CTE mismatches between different materials in the interface.

Little has been published in literature on the subject of reliability on CNT array TIMs with the exception of one ASTM D5470 based burn in test that was performed on a polymer infiltrated CNT/Al interposer [93]. By cycling the samples under temperature and mechanical load the authors were able to subject TIMs to simulated wear similar to that of real usage. However, the CNT interposer in that experiment was mechanically detached, thereby functioning like a thermal pad, and infiltrated using a polymer. Therefore, it bears little resemblance to the normal CNT array TIM that is mechanically attached on both ends of the array. To mend this gap in literature, parts of this thesis was dedicated to investigate the matter and to reach conclusions regarding design of CNT array TIMs.

In this thesis I present Paper C and Paper E that together form the first systematic studies on CNT array TIMs subjected to thermal cycling to address reliability concerns.

3.1 Preliminary Reliability Study

An initial trial of the reliability was conducted using the azide based CNT array TIMs from Chapter 2.3.2 which previously had demonstrated excellent performance in laboratory settings [85]. These samples were subjected to thermal cycling in order to investigate the lifespan of the system under simulated use. The thermal cycling test condition "B" from the JEDEC standard [135] was chosen, corresponding to a cycling between −55°C and +125°C, with a ramp time of 10 min and holding time at each extreme for 20 min continuing over 500 cycles in total. Although this cycling standard is a bit harsh for normal usage, it was still chosen as the intention of the research project was to place the CNT TIMs in fighter jet radars. The thermal resistance was evaluated at every 100 cycles using laser flash measurements and these results are presented in Figure 3.1.

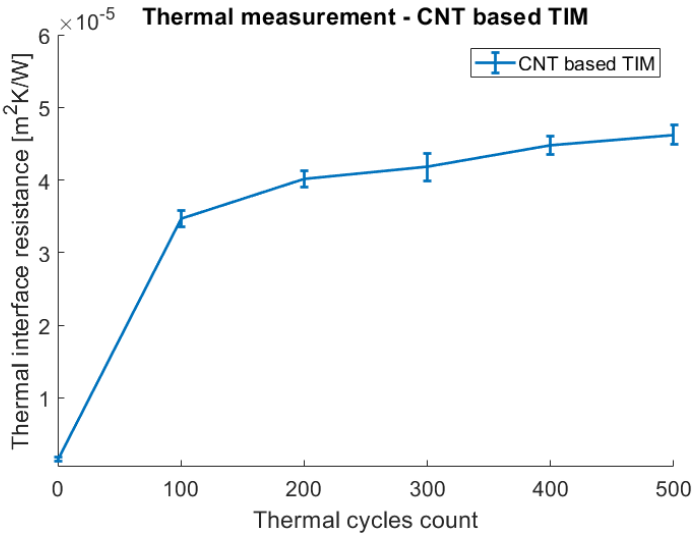


Figure 3.1: Results from the thermal cycling of the CNT based TIM interfaces.

Judging from the obtained thermal resistance results, the CNT array TIMs quickly deteriorated during thermal cycling and had increased its thermal interface resistance 20 times already after the first 100 cycles. This trend continued throughout the cycling at a lower pace and would after total 500 cycles end up with an increased thermal interface resistance of 27 times the original value. Unfortunately the measurement intervals chosen for this study was 100 cycles as most of the resistance increase occurs in between the first and the one hundredth cycle. It would be beneficial to know if the system goes through an abrupt break point right after the first couple of cycles or if it is a gradual increase of thermal resistance that later levels off. Three

possible weak points were hypothesised for the performance degradation: the HLK5 polymer coating, the CNT bulk and the catalyst side anchoring. In order to find the root of the observed reliability issues, it was apparent that further failure analysis was required to assess the reliability of the CNT array TIM system.

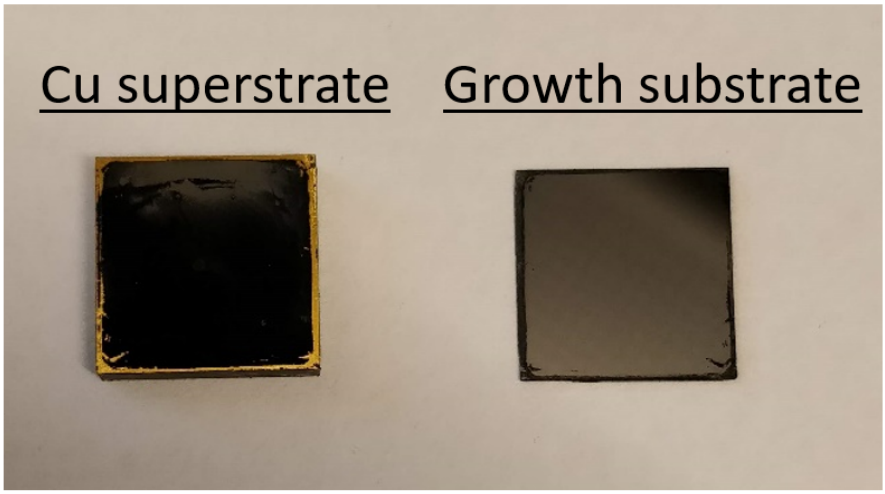


Figure 3.2: Delaminated CNT array TIM interface after thermal cycling.

All the investigated samples delaminated at some point, during or immediately after cycling and once they did they all released on the growth substrate side of the interface, as seen in Figure 3.2. This indicates that the weak point of the interface resides on the CNT root side and not on the polymer coating side. However, even if no degradation could be observed of the HLK5 coating, further studies are still required to evaluate the long term effect usage would have on the polymer in a TIM application.

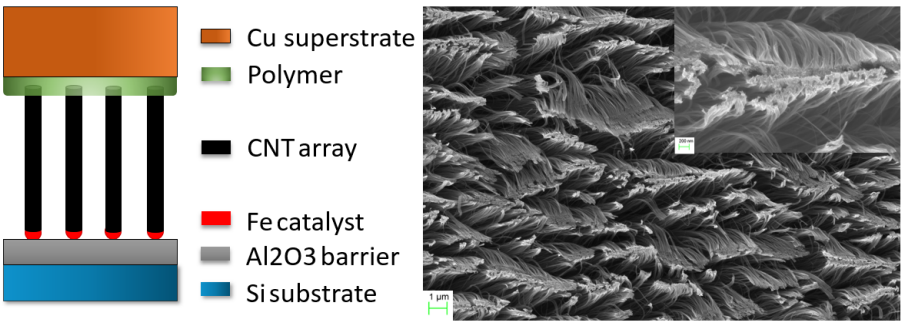


Figure 3.3: Left side: Cross section of the CNT array TIM showcasing the materials involved. Right side: SEM image of the delaminated CNT array.

The samples were analysed after delamination using SEM and XPS in order to further investigate the failure mode. The left side of Figure 3.3 illustrates the different components of the interface and the right side of Figure 3.3 show an SEM image of the backside of the Cu heatsink after delamination. One of the hypothesised failure modes was that the CNT array would break along the CNT strand which would leave a part

of the CNT array on the growth substrate. In this case however, the array clearly was completely uprooted from the Si substrate. This means that the weakest link of the interface that needs further examination is the CNT/Fe/Al_2O_3 anchoring. In this case the issues could either stem from chemical degradation or purely from the shear forces that arises from the CTE mismatch between the Si and Cu substrates. In order to separate those two effects, free-standing CNT arrays were measured before and after cycling using the PPR method. This way the thermal interface resistance on the catalyst side of the array could be assessed without any CTE mismatch related effects.

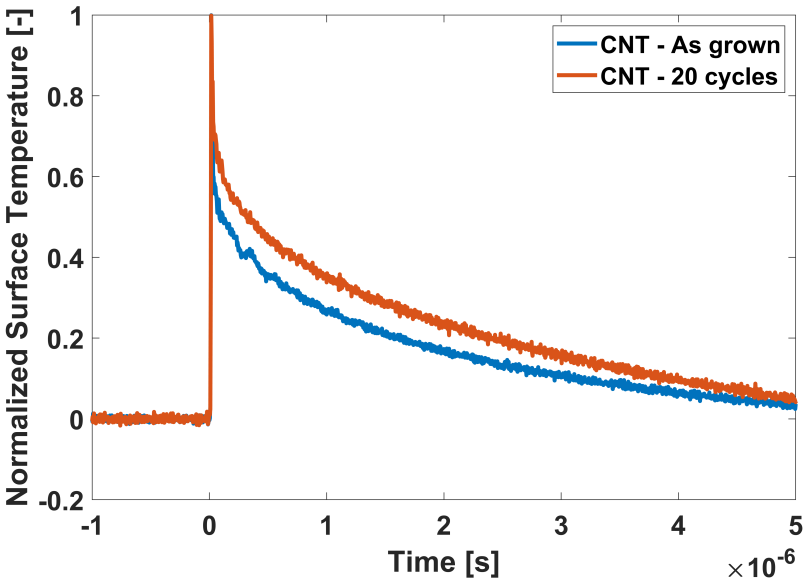


Figure 3.4: PPR measurement data from an accelerated aging test done on freestanding CNT arrays grown on Si substrates.

The results from the PPR measurement found in Figure 3.4, show that the interface contact resistance had increased by almost 140 % already after 30 cycles. As the contact resistance should reside solely in the CNT/Fe/Al_2O_3 link, this is a strong indication that the mechanical anchoring of the CNTs degrades during usage. By investigating thermal reliability aging on free standing CNT arrays any CTE mismatch related effects should be removed. Therefore, the increased thermal interface resistance seen in Figure 3.4 should be directly tied to deterioration of the catalyst anchor point where the CNTs are connected to the growth substrate. This hypothesis was scrutinized further using XPS analysis on both the Si substrate as well as the Cu heat sink after delimitation of the original interfaces. The results from this study is presented in Figure 3.5a and 3.5b.

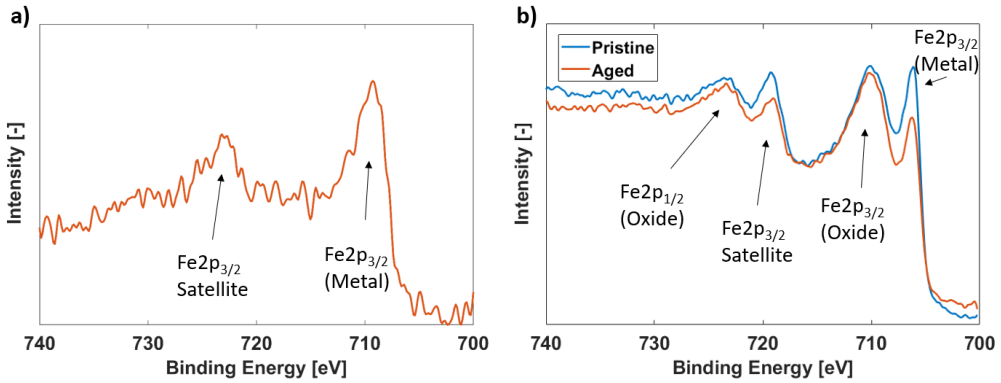


Figure 3.5: XPS spectrum acquired from the delaminated parts of a CNT array TIM after thermal aging: a) Si side, b) Cu side.

As seen in Figure 3.3, the CNT strands are attached to the Si substrate via an Fe particle that in turn resides on an Al_2O_3 thin film. If the connection is stronger between the CNT and Fe particle than the adhesion between the Fe particle and the Al_2O_3 layer, the Fe particles should follow the CNT roots during delamination. This would mean that it would be possible to find Fe particles on the backside of the Cu heatsink. This was investigated and the XPS spectrum is shown in Figure 3.5a. As seen, there was indeed a Fe2p signal present in the spectrum which indicates that the CNT/Fe bond is strong enough to remove the Fe particle from the Si substrate. By comparing a delaminated Cu sink after accelerated aging to an unaged and mechanically sheered Cu sink, the effects of aging could be compared in terms of present Fe particles still attached to the CNT roots. Analysis of the Fe2p and C1s peaks in the XPS spectrums from the two samples show a 70% decrease of Fe particles on the sample that had gone through accelerated aging. Furthermore, the Si substrates were analysed in the same way and the Fe2p peaks from the XPS spectrum of the two samples are compared in Figure 3.5b. By comparison the aged sample had 15% lower amount of metallic Fe compared to the Fe oxide peaks. These results seems to align well with the hypothesis regarding chemical degradation during accelerated aging and was therefore investigated further in Chapter 3.4.

The results presented in Paper C indicated that thermal cycling degrades the CNT/catalyst adhesion considerably. Two hypothesises were developed, either the degradation came from a pure CTE mismatch induced shearing of the CNTs in the interface or a chemical effect on the CNT anchor point on the Si substrate. By isolating the system to focus on chemical effects we showed indicative results of oxidation that resulted in a weaker link in-between the CNTs and the Si substrate. Consequently, this would explain the dramatic increase in thermal interface resistance as well as the degradation of mechanical integrity observed during the thermal cycling. However, the CTE mismatch might still be an issue that has to be taking into account when assessing the reliability of the system and this aspect was studied further in Chapter 3.2 and 3.3.

3.2 Array Length Impact on Reliability

To empirically test how the CNT length affects the reliability of CNT array TIMs, a new batch of samples were fabricated and subjected to a shorter accelerated aging test. This test was according to the thermal cycling protocol described in Chapter 3.1 and performed over 50 cycles. The new samples were bonded using a 1 µm thick In layer [136] to attach the CNT arrays of different lengths in between a Cu sink and the Si growth substrate. The CNT arrays were grown in lengths of 10, 50, 80 and 200 µm and prepared before In bonding with a sputtered Ti/Au metallization of 10/20 nm thickness. Images of the as-grown CNT array, CNT tips after metallization and a cross section of the bonded CNT array TIM is presented in Figure 3.6.

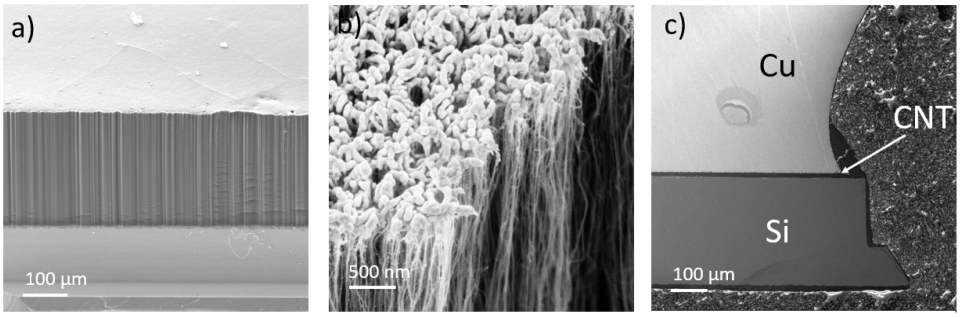


Figure 3.6: SEM images of the CNT array TIM before and after bonding: a) 200 µm long CNT array after growth. b) Top-side view of CNT tips after metallization. c) Cross section of the bonded CNT array TIM which reveals the BLT of the interface.

Figure 3.6c shows a 50 µm long CNT array that was bonded as a TIM which in the process compressed the array down to a 15 µm BLT. This compressibility of a CNT array is of dependent on bonding pressure and array density and is therefore different for each design. However, the settings used for the In bonded CNT array TIMs fabricated in this thesis was determined to yield a BLT corresponding to 30 % of the original CNT array length.

The thermal resistance degradation of the fabricated samples was monitored before cycling (0th cycle) as well as at cycle steps 5, 10, 20 and 50. The collected results are presented in Figure 3.7. The thermal interface resistance results in Figure 3.7a shows how the different CNT height settings affects the performance degradation. As seen, the initial thermal interface resistance is also dependent on the array length according to Equation 1.3. In other words, a longer CNT array yields larger starting resistance and a slower resistance degradation and the other way around. To visualize the performance degradation clearly, each curve from Figure 3.7a was exponentially fitted according to the equation:

$$R_{th} = A \cdot ln(n) + B \tag{3.1}$$

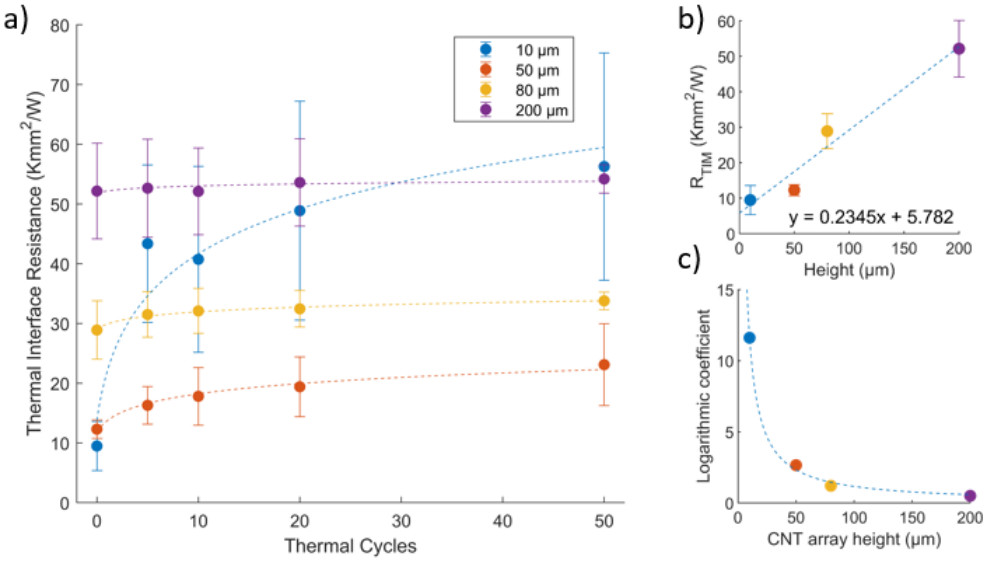


Figure 3.7: a) Thermal interface resistance plotted to number of thermal cycles together with trend curves for the different CNT array heights of CNT array TIMs. b) Thermal interface resistance before thermal cycling to array height. c) Logarithmic constant from the trend curves in a) plotted to CNT array height.

Where R_{th} is the thermal interface resistance, A is a constant, n is the total number of cycles and B is equal to R_{th} at n = 0. Figure 3.7b presents the first measured resistance value at 0 cycles and is plotted for each of the samples together with a linear fitting curve. The constants describing this trend curve gives the contact interface resistance $R_{C1} + R_{C2} = 5.782$ mm^{2}K/W and the bulk conductivity $\frac{1}{0.2345} = 4.26$ W/mK. The high contact resistance and low thermal conductivity of the interfaces are tied to the employed indium bonding solution which fails to contact enough CNTs in the array compared to the azide based CNT array TIM discussed in Chapter 2.3.2. However, the CNTs are demonstrated to bond equally over the whole interface which is important for the results to be relevant in a general CNT array TIM reliability context. The logarithmic constant A for each of the curves are plotted together in Figure 3.7c. As seen, the performance degradation is proportional to the CNT length which is expressed as a quicker leveling of performance degradation, lower logarithmic constant and higher starting resistance with longer CNTs used. The data were fitted according to:

$$A = \frac{C}{L_{CNT}} \tag{3.2}$$

Which describes the relation between the logaritmic constant in Equation 3.1 and the original CNT array height L_{CNT}. From this equation and the data presented in Figure 3.7c we can extract the constant C = 116.4. Taking this a step further, we can simplify Equation 3.1 into $\Delta R_{th} = A \cdot ln(n)$ and combine it with Equation 3.2:

$$L_{CNT} = \frac{C}{\Delta R_{th}} \cdot ln(n) \tag{3.3}$$

The resulting equation gives the required CNT array length for a system described by C and a certain absolute thermal interface resistance degradation over n thermal cycles. This equation can be used to compare our system to reasonable demands from commercially available TIMs. Thermal grease for example is expected to degrade about 2 - 3 times over 1000 cycles [137] and state-of-the-art CNT array TIMs can offer about 2 mm^2K/W [19]. This gives us: $\Delta R_{th} = 2$, n = 1000 and C = 116.4 which calculates to $L_{CNT} = 402$ µm. In other words, the required CNT array length is much larger than the commonly featured CNT array TIM designs found literature that employ 10 - 30 µm long CNTs.

Many of the parameters that determine C from Equation 3.3 can be derived from the CTE mismatch induced sheering the CNT array TIM is exposed to at elevated temperatures. The relative displacement δ, that arises due to the CTE mismatch between the substrates in a TIM can be calculated using the following equation:

$$\delta = \Delta T \cdot \Delta\alpha \cdot DNP \tag{3.4}$$

Where ΔT is the temperature difference the system is subjected to from the relaxed state (usually curing temperature), $\Delta\alpha$ is the CTE mismatch between the joined substrates and DNP is the distance to neutral point which is illustrated in Figure 3.8a.

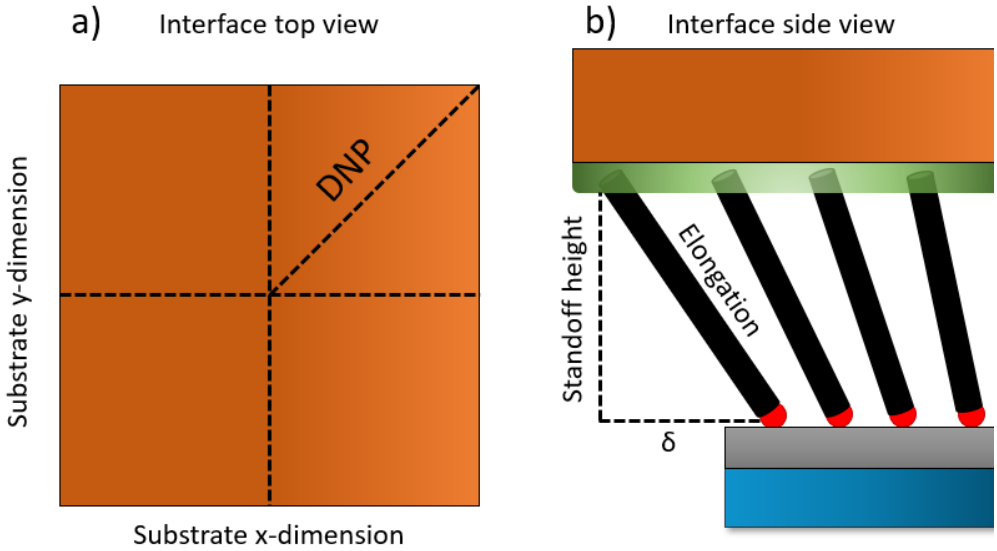


Figure 3.8: CTE induced shearing effect on the CNT array TIM: a) distance to neutral point on a substrate, b) elongation of the CNTs in the interface during temperature cycling.

DNP for square shaped substrates can be calculated according to $DNP = \frac{\sqrt{2}\ell}{2}$. Since the CNT in the CNT array TIM is connected at the tip and root at the respective substrate they should be regarded as mechanically free in the horizontal plane and restricted in the z-plane. This means that relative displacement between

the two connected substrates will stretch and elongate the CNTs in accordance with Figure 3.8b. The effective elongation S of the CNT will be dependent on the relative displacement δ and the standoff height L_{BLT}. This stretch effect will be zero at the neutral point in the middle of the two substrates and increases proportionally out on the side. As the relative displacement δ, standoff height and the elongated CNT forms a right-angled triangle, the stretch effect can be calculated using the Pythagoras theorem:

$$S = \sqrt{\delta^2 + {L_{BLT}}^2} = \sqrt{\left(\Delta\alpha\Delta T\frac{\sqrt{2}\ell}{2}\right)^2 + {L_{BLT}}^2} \tag{3.5}$$

The values associated with the CNT array TIM samples from the length study are: ΔT = 180°C, ℓ = 8 mm, $\Delta\alpha$ = 14 ppm/°C and a standoff height that correspond to 30 % of the original CNT length (according to Figure 3.6. The calculated stretch is then: 146, 41, 35 and 31 % for the 10, 50, 80 and 200 µm samples compared to the total original CNT length.

Depending on how the CNTs connects to the interface there will be more or less room to buffer the CTE induced stress applied on the interface. If only the tips of the CNTs are connected at the interface all compression during interface closing would cause the CNT to curl like springs in the bulk. Another way sees the CNTs fold on the interface causing more of the same CNT to physically bond to the interface. In the first case we should assume that the interface can buffer stress at least up to the full original CNT array length without any additional strain being applied to the CNTs. In the second case the CNTs would be locked in place and any further stress would have to be buffered by the CNTs themselves. However, in reality the CNT are probably connected somewhere in between these two extremes [138]. This means each CNT array TIM will be different as the closing process will determine how much of the CNT that will be locked in contact with the bonding surface.

Studies have shown that CVD grown CNTs possess spring like properties of around 3 - 5 % [139] elongation at break and up to 20 % from theoretical modelling work [140, 141]. However, the mechanical strength of the bulk CNT walls does not seem to be a weak point in this study since none of the CNT actually brakes in the middle of the strand. Instead, the main focus should lie on the covalent anchoring between CNT and the catalyst particle as well as the adhesion of the catalyst particle to the growth substrate. Once this bottleneck is removed, further studies related to the mechanical properties of the CNTs themselves are justified.

These results demonstrate that there is a direct trade-off between performance and reliability of a CNT array TIM type system and that the interfaces requires careful design before an optimal balance between the two can be obtained.

3.3 CTE Mismatch Induced Delamination

The relative impact of CTE mismatch and chemical degradation on the reliability of CNT array TIMs can be studied by isolating the two effects in different TIM designs. This was done in a study with grown CNT arrays of 80 µm, bonded using the In method (from Chapter 3.2) in 4 different interface configurations. As CTE mismatch appears when materials with different thermal expansion are joined, this effect can be circumvented by for example bonding the Si growth substrate with another Si substrate. The chemical degradation effect that was discovered in Chapter 3.1 was determined to reside in the catalyst anchor points and is therefore possible to remove by transferring the array making it a double side bonded interface (as outlined in Chapter 2.3.3). The new samples were subjected to accelerated aging by thermal cycling over 500 cycles using the same conditions as in Chapter 3.1. The 4 different configurations, SSi, DSi, SCu and DCu are illustrated in Figure 3.9.

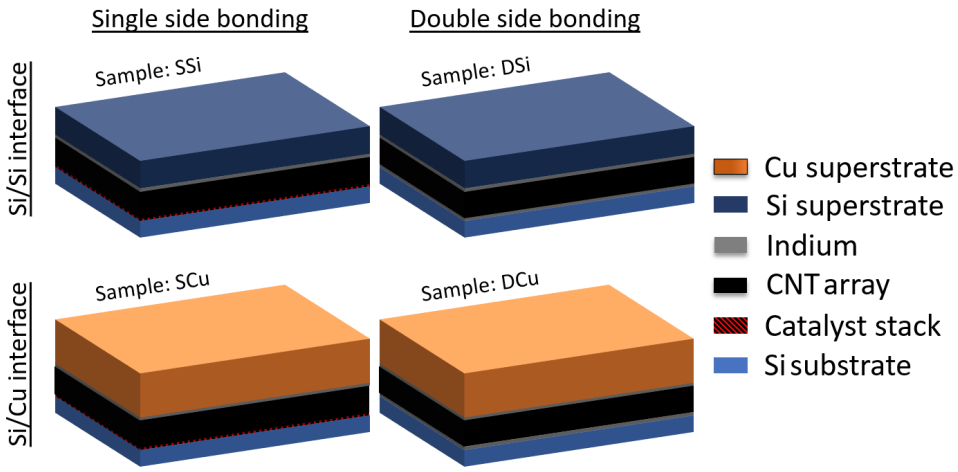


Figure 3.9: Four different interface configuration used for the thermal cycling: SSi - single side bonded Si/Si interface, DSi - double side bonded Si/Si interface, SCu - single side bonded Si/Cu interface and DCu - double side bonded Si/Cu interface.

The first two types of interface configurations, SSi and SCu were fabricated using a flipchip bonder. Both were bonded using the Si growth substrate with the grown CNT array together with a Si and a Cu substrate respectively, resulting in two samples with catalyst anchor points with and without the CTE mismatch (Si/Si, Si/Cu). In the case of DSi and DCu, the growth substrate was removed before cycling by shearing and replaced with a new Si substrate coated with an In interface. This would result in two configurations without the catalyst anchor points, with and without CTE mismatch. In this way, the impact of the two effects could be isolated. The thermal interface resistance was measured using the laser flash method and the results are presented in Figure 3.10.

The results from the accelerated aging study show a clear trend where samples from the DSi and SSi series are stable over the 500 cycles. In the case of DCu the results vary over the 500 cycles but seems stable which could be an indication that the reliability of the measurement somehow has been affected from the

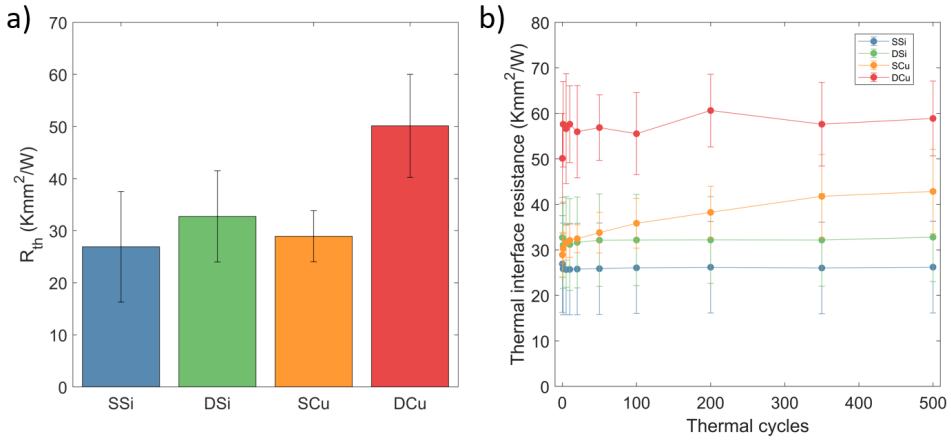


Figure 3.10: Results from the thermal cycling study on the 4 different types of CNT array TIM configurations based on 80 µm CNTs: a) Initial values of the measured resistance in a histogram graph, b) scatter plot of the thermal resistance development over the 500 thermal cycles included in the study.

sample transfer. This might be due to an increased contact resistance that is associated with the Cu substrate roughness. In the case of SCu we can see a clear logarithmic trend equal to that demonstrated in the array length study in Chapter 3.2. These results show that reliability of the CNT array TIM will be improved significantly by removal of the CTE mismatch. Unfortunately, the results from DCu are too unreliable to draw any definite conclusions regarding the strength of the CNT array contacts in the double bonded In configuration. The bonding strength should however be increased which in turn could be enough to improve the reliability in Si/Cu bonded CNT array TIMs. Finally, no clear signs could be identified in this study that links performance to chemical degradation of the catalyst anchoring. This however, could simply be due to the larger thermal interface resistance values seen in this study compared to the preliminary study in Chapter 3.1.

3.4 Catalyst Degradation

Even though no clear signs on chemical degradation could be seen in Chapter 3.3 it is still of interest to analyze the catalyst before and after the accelerated aging test. As seen in Chapter 3.1, a significant increase in thermal interface resistance could be attributed to chemical oxidation of the Fe catalyst particles. However, if this effect is sufficient to affect the covalent bonds between the catalyst particle and CNT strand requires further studies [142]. Chemical analysis of the samples was conducted using XPS and is presented in Figure 3.11.

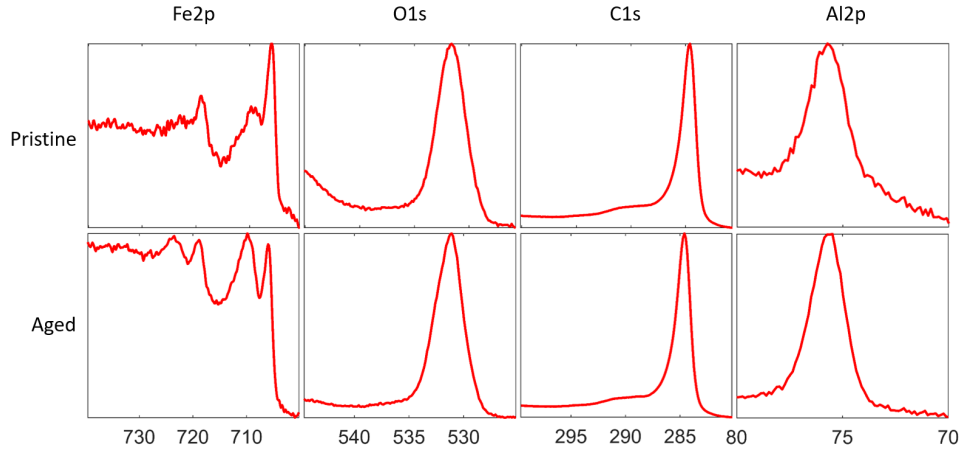


Figure 3.11: XPS multiplex scans of each of the elements found on the Si growth substrate after delamination.

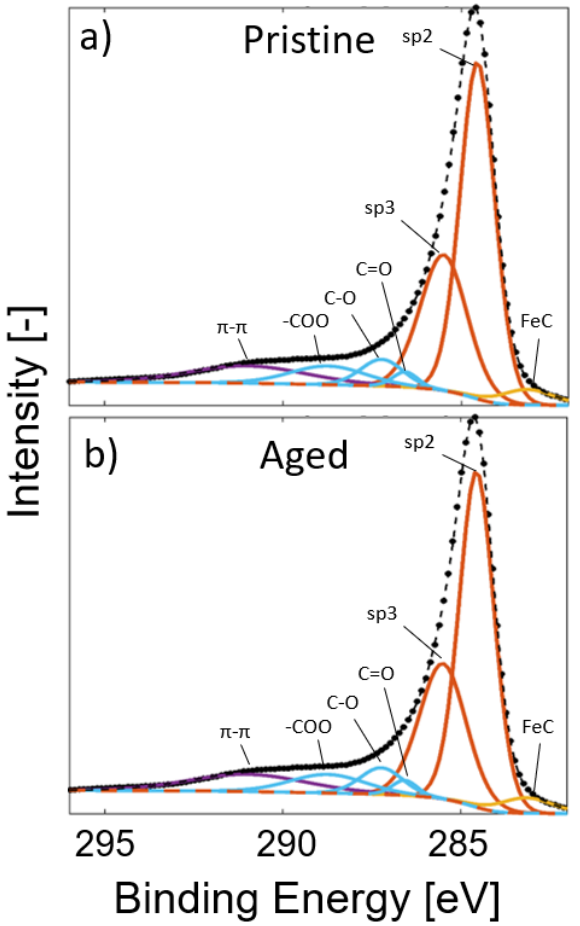
As expected the obtained spectra before and after aging showed clear peaks in positions related to: C, O, Al, Si and Fe. The Si signal was quite weak and there was no anticipated effect related to the aging, so the Si peak was discarded in this study. The remaining peaks were all related to the CNT/Fe/Al_2O_2 contact that the study from Chapter 3.1 concluded to be of interest. As seen, the only peak that shows clear signs of chemical change is the Fe2p peak, otherwise Al2p, O1s and C1s looks largely the same. A chemical quantification of the relative peak areas based on the spectra in Figure 3.11 is presented in Table 3.1.

(wt%)	Fe2p	O1s	C1s	Al1s
Pristine	0.12	4.68	93.25	1.95
Aged	0.20	5.32	91.28	3.20

Table 3.1: Elemental composition of CNT catalyst layers as determined from XPS data in figure 3.11

According to the hypothesis drawn from the preliminary study in Chapter 3.1, chemical oxidation of the Fe paricles would result in a deteriorated bond strength to the CNT root. As a consequence, this was believed to result in a higher concentration of remaining Fe particles on the growth substrate after delamination after compared to before accelerated aging. As seen, this effect was reproduced again in this study where all concentrations would increase in the case after aging compared to the pristine sample. This could mean that more carbon would remain on the growth substrate which in turn would give lower numbers for the other elements. However, by isolating the Fe2p and C1s peaks there is still about double amount of Fe particles present on the growth substrate after delmination in the aged sample compared to the pristine case. This result confirms our original hypothesis about the chemical degradation of the Fe catalyst particles in the CNT array TIM.

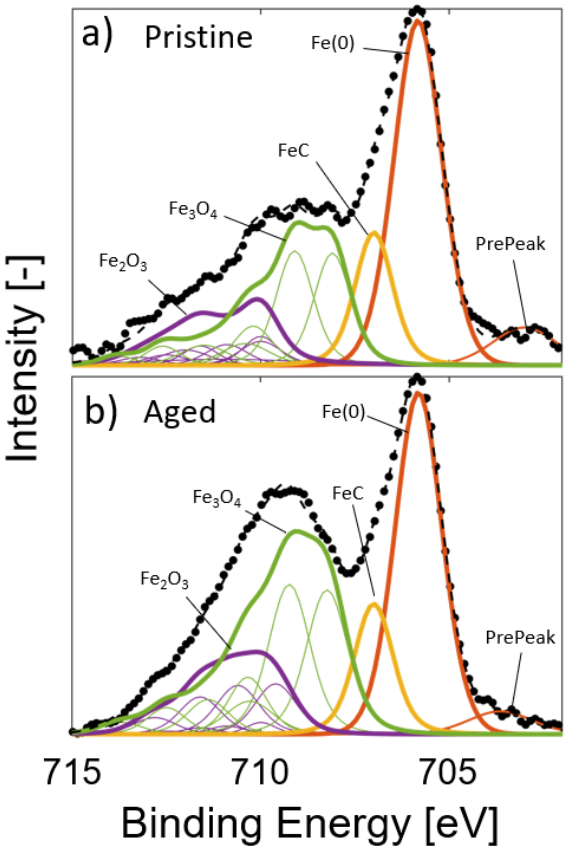
It was necessary to take a more careful look at the CNT/Fe/Al_2O_3 system in order to learn more about the chemical effects from accelerated aging. Therefore, the C1s and Fe2p peaks were analysed further through peak fitting. These results are presented in Figure 3.12 and 3.13.



(at%)	Pristine	Aged
sp2	52.57	56.81
sp3	21.59	18.47
π-π	9.09	7.36
FeC	2.71	3.27
C-O	5.16	4.69
C=O	5.48	6.09
-COO	3.41	3.32

Figure 3.12: Peak fitting results from the C1s data acquired from the Si growth substrate before and after accelerated aging.

In the case of the C1s peaks, four main types of peaks could be identified: the C-C peaks that correspond to sp^2 (C-C) and sp^3 (C=C) bonded carbon, C-O peaks like single and double bonded oxygen as well as carboxylate groups (-COO), carbides which in this case was mainly the iron carbide specifically and finally a small contribution from the $\pi - \pi$ stacked orbitals. The relative amount of oxygen bonded to carbon and sp^2/sp^3 is related to the crystallinity of the CNTs and will therefore differ from sample to sample. Nevertheless, these results indicate an increase of FeC in relation to the sp^2 peak which would imply a higher amount of Fe catalyst particles on the growth substrate after aging.



(at%)	Pristine	Aged
Fe(0)	38.18	32.35
FeC	19.77	16.17
Fe_2O_3	26.24	30.68
Fe_3O_4	15.80	20.80

Figure 3.13: Peak fitting results from the Fe2p data acquired from the Si growth substrate before and after accelerated aging.

The Fe2p data were also peak fitted for further analysis which is presented in Figure 3.13. In this case four different groups of contributing signals were taken into account: metallic Fe (Fe(0)), iron carbide FeC and the two different types of iron oxides Fe_2O_3 (alpha and gamma phase - Fe^{3+}) and Fe_3O_4 (Fe^{2+}, Fe^{3+}) [143]. A 'pre-peak' was also identified which is associated with defects in the iron phase [144]. Other contributions that were neglected includes hydroxides as the materials are in solid phase and FeO (Fe^{2+}) due to its instability at room temperatures which in turn causes it to combine into Fe_3O_4 [145]. In the case of iron oxides there will appear a group of peaks due to the phenomena called multiplet splitting which takes into account in the peak fitting procedure which is included in Figure 3.13. Each of the multiplets was then summarized into a group of peaks that was used for the elemental comparison. As seen, the metallic iron and iron carbide concentrations are lower after aging. The iron oxide species have, on the other hand, grown in concentration. These values only take the iron signal into account which makes the effect with higher iron concentration after aging, seen in Figure 3.12, no longer possible to observe. Additionally, the data suggests that the iron carbide phase is consumed by the oxide growth which should imply that the covalent contact between the CNT and Fe catalyst particle ultimately will break. This result aligns well with the previous observation where the iron concentration would decrease after aging on the CNT root side from Chapter 3.1.

The deterioration of the carbide phase on the Fe catalyst particles is also interesting for a different reason. A controlled oxidation of these particles could enable an efficient route to release CNT arrays from their growth substrates. Usually CNT arrays are deformed during transfer since that process both involves compression and sheering. Instead, the oxidation route could facilitate a deformation free transfer method for CVD grown CNT arrays.

3.5 Conclusions

The reliability study of CNT array TIMs shows a clear relation between CTE mismatch, CNT length and thermal interface resistance degradation. This is interesting as the majority of published work on these kinds of interfaces used CNT array lengths of 10 µm, which is far shorter than what would be required in order to compensate for the CTE mismatch of said interfaces. A closer look at the failure mode of our interfaces reveal that the connection between the CNT and the iron deteriorates during accelerated aging through chemical oxidation.

The goal of this study was to investigate the reliability for CNT array TIMs and to derive design guidelines that can direct future research and development on the subject. Based on our findings the following was concluded:

- Thermal expansion induced strains must to be balanced with a CNT array of sufficient length for thermal interface resistance to be sustained.
- The weakest link in the interface was determined to reside in the catalyst particle anchoring point of the CNTs to the growth substrate. Reliable interfaces proven up to 500 thermal cycles were obtained by transfer and double bonding.
- A noticeable resistance degradation effect was discovered in interfaces solely due to chemical oxidation of the catalyst particles.

These results demonstrate that good reliability can be ensured and that these types of materials provide a good compromise between performance and reliability.

Chapter 4

Carbon Nanomaterials for Interconnect Applications in 3D Integrated Circuits

The exponential performance trend of ICs and digital circuits known as Moore's Law has been possible due to the direct relation between profitability, performance and physical dimensions [1]. Since the '60s, semiconductor processes have been developed from a design node of 50 µm down to the current state-of-the-art of 5 nm [26]. The obvious result of this development enables developers to pack more transistors in silicon packages every year at a lower fabrication cost. However, this also means that the interconnects used to route signals and power between transistors scale as well. This way, traditional 2D packaging methods for VLSI are soon obsolete as miniaturization costs escalate at process nodes below 10 nm [146]. Therefore, 3D packaging is seen as a profitable solution going forward [9]. The development of 'non-Cu' interconnects is seen as a key driver to facilitate 'More Moore' progression for CMOS devices. Such an industry standard replacement for Cu should provide improved properties in terms of lower capacitance, resistivity, ampacity and CTE mismatch. That way, improved power efficiency, RF performance, signal noise and delay as well as reliability can be achieved for the next generation of 3D packaged CMOS devices [29].

Low dimensional carbon nanomaterials are proposed for use as interconnects due to their unique electrical properties [147]. Graphene and CNT based materials are ideal for interconnect applications due to their favorable properties i terms of resistivity, ampacity, lack of skin effect and low parasitic capacitance [148–150]. However, a replacement material for Cu interconnects also needs to be future proof for a continued scaling. In the case of Cu, the main limitation is found at the MFP limit around 40 nm [35]. As a result, miniaturization beyond this point will cause unfavorable resisitivty and capacative escalation. By switching to graphene and CNTs which have a much longer MFP in the order of 10^3 nm, a directed propagation of electrons along the structure can be achieved which reduces the grain boundary scattering [150, 151]. This effectively bypasses the MFP limitation of Cu and would allow graphene and CNTs to scale for a foreseeable future. Therefore, low dimensional

nanocarbon materials have the potential to solve many of the issues found in modern CMOS devices.

In this chapter, two low dimensional carbon nanomaterials have been explored for vertical and horizontal interconnect applications. Horizontal graphene interconnects are fabricated through a novel method outlined in Paper F and a Cu/CNT composite for vertical TSVs that is demonstrated in a 3D test architecture is presented in Paper G

4.1 Repeated Synthesis of Graphene using a Pre-Dissolved Carbon Source

Interconnects made out of graphene have been demonstrated by mechanical exfoliation [152], epitaxially grown [153] or chemically derived [154]. However, none of these methods are economically viable or practical for high quality graphene interconnects aimed towards VLSI fabrication [155]. Graphene fabrication can also be achieved using CVD processes. This way, graphene made out of grains up to several micrometers can be obtained in a reproducible fashion.

Graphene growth using CVD works in a similar way to that of CNTs but uses foils of transition metals as catalyst to grow from. The catalyst foil works by breaking down a hydrocarbon precursor gas and subsequently reorganize the disassociated carbon atoms into the hexagonal lattice structure of graphene on top of the foil. A few different metals that have been investigated for graphene CVD synthesis and the most usual ones are: Ru, Ir, Pt, Co, Ni and Cu to name a few. These metals differ in growth potential due to their different attributes in terms of carbon solubility, bonding strength to carbon and crystal structure. Out of these, Cu and Ni have been demonstrated with commercial success [156].

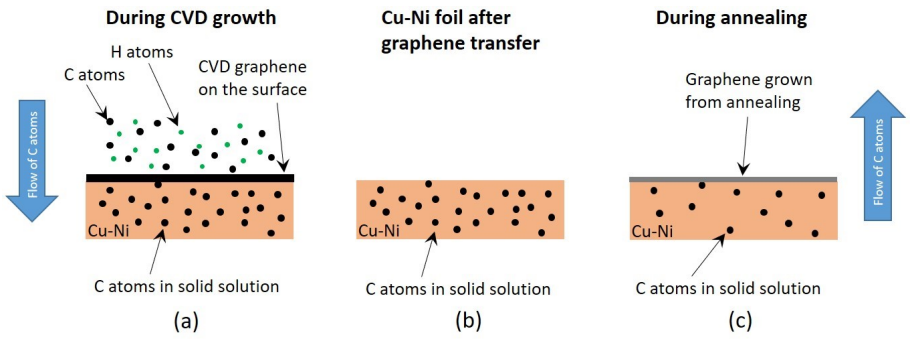


Figure 4.1: Graphene growth on Cu-Ni foil using the CVD method: a) Carbon pre-cursor gas is supplied into the reactor causing it to dissolve into the foil and exfoliate out on the foil surface. b) Foil after graphene transfer retains dissolved carbon available for graphene exfoliation. c) Additional graphene can be synthesised by annealing.

Standard graphene fabrication through CVD on Cu foils gives high quality mono-layer graphene due to the low C absorption in Cu [157]. The alternative, Ni, is also used but is less convenient as the carbon absorption is higher and results in inferior quality and additional graphene layers [158, 159]. In theory, an engineered foil composition could facilitate a high carbon absorption while still only exfoliating mono-layer graphene [160]. That way, the foil should be able to exfoliate mono-layer graphene several times without the need for additional precursor gases as sufficient amounts of disassociated carbon is absorbed in the foil. An illustration of this process is found in Figure 4.1.

This principle was tested by using a foil composed of 55wt% Cu and 45wt% Ni as catalyst material for CVD graphene growth. The foils were washed using acetic acid to remove native oxides before thermal CVD growth. After each of the growth cycles (including CVD growth) the foil was covered with a graphene layer that could be transferred by normal methods. Transfer was done through the bubbling method to silicon chips with thermal oxide for optimal graphene contrast [161]. Following the first transfer, the foil could be annealed several more times, each time revealing new graphene layers. This process could in theory be repeated as many times as the carbon concentration in the foil allows. The process is illustrated in Figure 4.2.

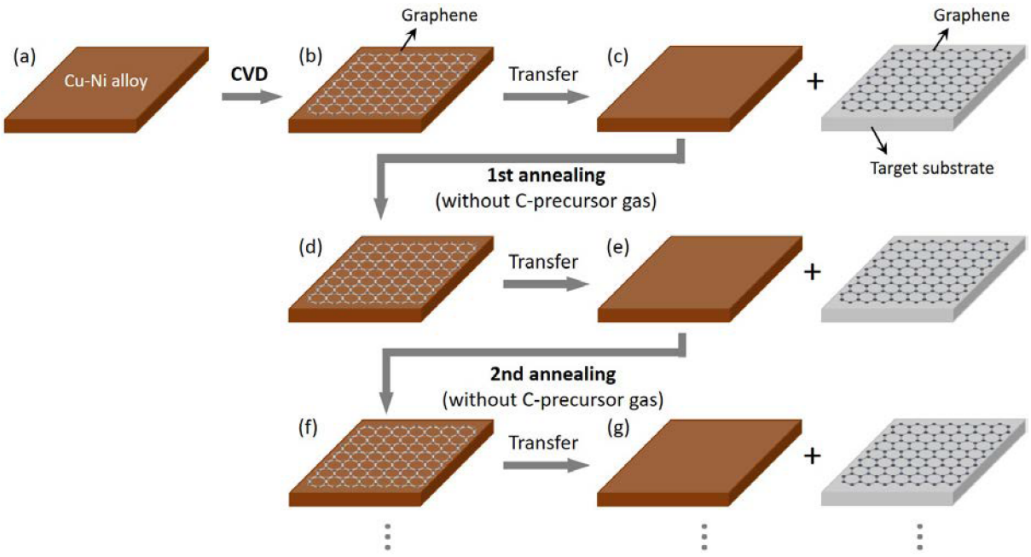


Figure 4.2: Repeated graphene growth from Cu/Ni foils. a) - c): normal graphene CVD growth process, d) - e) and f) - g): repeated annealing of the catalyst foil can reveal new graphene films without additional use of hydrocarbon source.

The process was repeated on several foil strips and the resulting graphene films were transferred over to Si chips in batches up to five consecutive annealing cycles. This resulted in a total amount of 6 graphene films per foil including the foil from the first CVD growth. Microscope images of the sample surfaces and a histogram of different graphene qualities on the Si chip is presented in Figure 4.3.

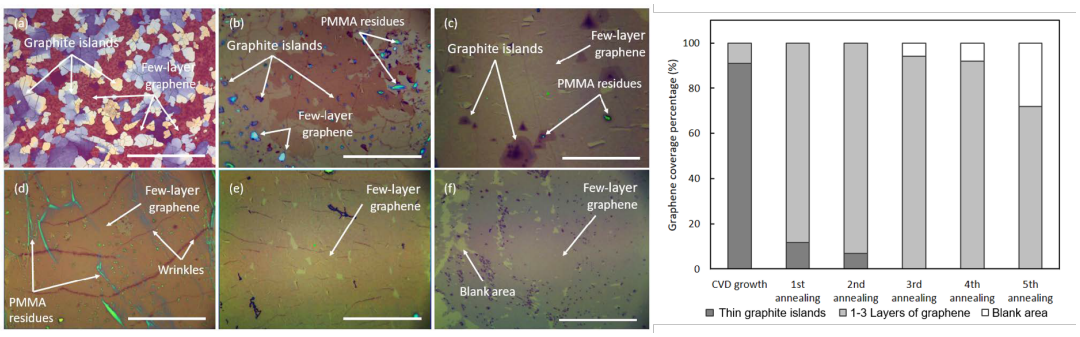


Figure 4.3: Left side image: Microscope images of the resulting graphene films from a) normal CVD growth, b) 1st annealing, c) 2nd annealing, d) 3rd annealing, e) 4th annealing, f) 5th annealing. Right side image: percentage coverage of different graphene qualities over the Si surface.

As seen, the microstructure picture of the first CVD grown graphene in Figure 4.3 a) show graphite islands and few layer graphene in-between. The overall coverage on the chip amounts to about 90 % graphite on the chip surface. Concentration of graphite islands is drastically decreased in the first and second annealing cycles, seen in Figure 4.3 b) and c), in favor of few layer graphene (1 - 3 layers). The occurrence of graphite islands disappears and the total coverage on the Si chips starts to decline in samples from the third up to the fifth annealing cycles, seen in Figure 4.3 d) to f). This behaviour is expected as the carbon content in the foil gradually depletes along the repeated annealing cycles. Further analysis of the graphene growth for every annealing cycle was done using Raman spectroscopy and is presented in Figure 4.4.

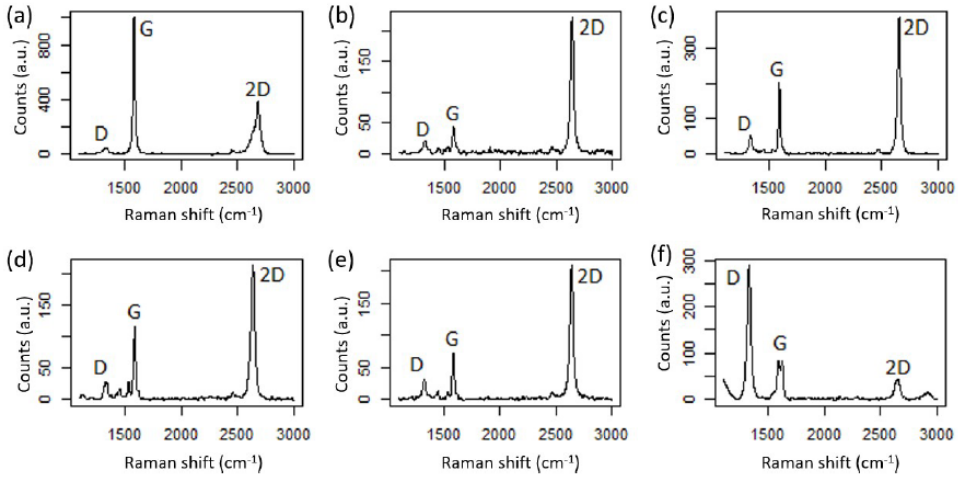


Figure 4.4: Raman spectrosopy results from measurements on the graphene surfaces on the samples: a) CVD grown, b) first annealing, c) second annealing, d) third annealing, e) fourth annealing and f) fifth annealing.

Raman measurements of the fabricated graphene coatings were done and the D, G and 2D peaks from the obtained data in Figure 4.4 was analysed. The D/G peak ratio of the first CVD grown graphene is much higher than of the consecutive

growths. This indicates that the graphene layers on the surface of the chip contains a low amount of defects. The graphene obtained at this growth cycle also contains a higher amount of layers as indicated by the 2D/G peak ratio. The Raman analysis of the graphene samples from the first to fourth consecutive annealing cycles (Figure 4.4 b) - e)) show similar trends in respect to quality and number of layers present. However, the defect concentration has increased and the number of graphene layers are fewer. Finally, the last annealing cycle in Figure 4.4 f) breaks the trend with a drastic increase of defects and much lower 2D/G ratio which in this case points at a depletion of carbon in the foil. This in turn prevents the foil from forming complete graphene layers and constricts further graphene synthesis.

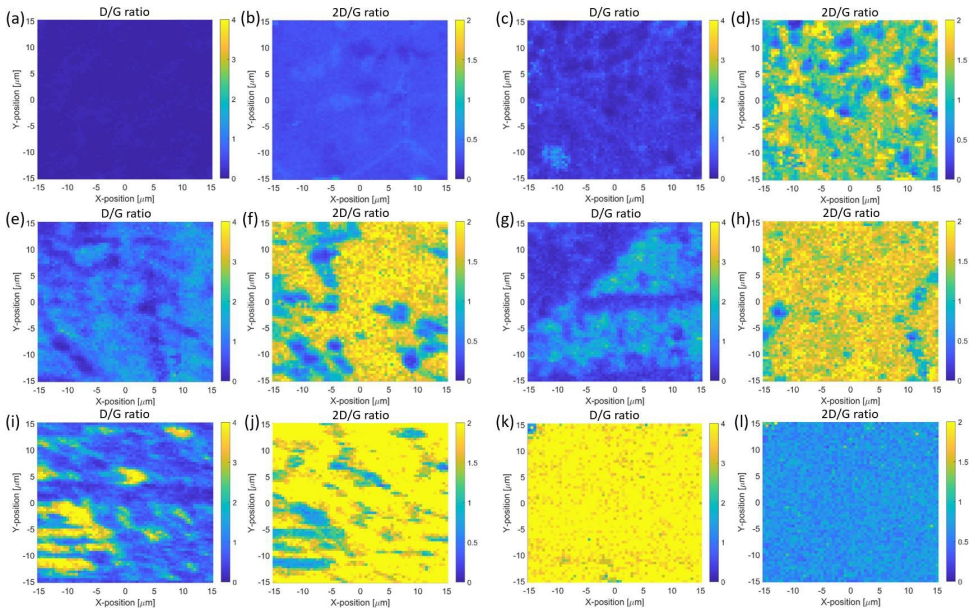


Figure 4.5: Raman mappings of a 30 by 30 µm area of the sample surface. Each set of mappings correspond to the D/G and the 2D/G ratio of a growth in the sample series: a) and b) CVD grown sample, c) and d) first annealing, e) and f) second annealing, g) and h) third annealing, i) and j) fourth annealing, k) and i) fifth annealing.

The trend from Figure 4.4 was confirmed to be consistent over large surfaces by Raman mappings covering areas of 900 µm^2. To efficiently make Raman mappings over larger surfaces, a few tweaks are necessary. In this case, the acquisition time was adjusted down to a fraction of a second and thereby enabling large area coverage with a small step length. This generally means that the individual scans become less accurate and more sensitive to external disturbances. However, when analyzing larger sets of data, especially when mapping a larger 2D area, anomalies can easily be filtered out before visualizing the data. The mappings illustrated in Figure 4.5 are built from about 4000 spectra each (65 by 61 steps) that in total took about 25 minutes to acquire.

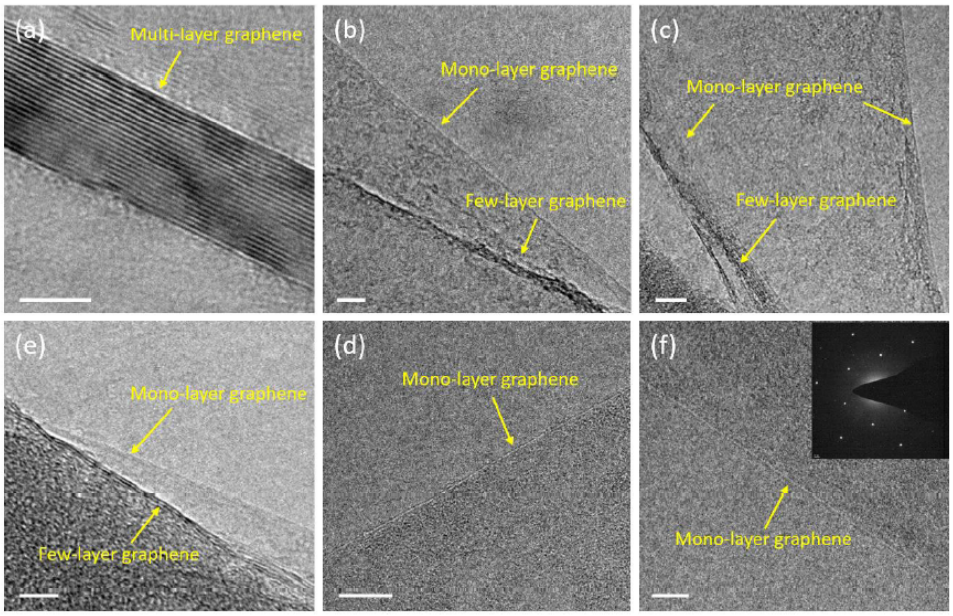


Figure 4.6: TEM images of the fabricated graphene: a) CVD grown, b) 1st annealing, c) 2nd annealing, d) 3rd annealing, e) 4th annealing, f) 5th annealing.

Further confirmation of the results from Figure 4.3, 4.4 and 4.5 was obtained using transmission electron microscopy (TEM), as presented in Figure 4.6. The number of layers each of the graphene films contained can be counted by locating a folded part of the film that can serve as an effective cross section. As seen in Figure 4.6 a), films grown using normal CVD growth yield a graphitic structure with the number of layers far exceeding what could be considered graphene. In the case of the 1st, 2nd and 3rd annealing samples in Figure 4.6 b) - d), no graphitic chunks can be found. These films instead consist mainly of few-layer graphene with smaller areas of single layer graphene. The last two annealing steps, 4th and 5th, found in Figure 4.6 e) and f) only contain single layered graphene.

The data from Figure 4.3, 4.4, 4.5 and 4.6 all show a graphitic structure being fabricated in the first CVD step with high quality. The 1st, 2nd and 3rd annealing cycles yield a few-layer graphene film with similar crystallinity. The 4th annealing cycle results in single layer graphene with decent coverage and the 5th and last annealing cycle fails to form a complete coverage of graphene. The differences seen in these results are related to the concentration of carbon present in each of the annealing cycles. Therefore, analysis of the concentration of carbon in the foil at each of the cycles can give insights in how the technology can be developed further.

The concentration of dissolved carbon was monitored using secondary ion mass spectroscopy (SIMS) on pieces of foil from each of the annealing cycles and this data is presented in Figure 4.7. This revealed that the carbon concentration reached up to 0.58 at% during the CVD growth. The carbon concentration decreased with repeated annealing cycles as carbon was extracted from the foil. This continued down to 0.42 at% after 3 annealing cycles, where the carbon concentration plateaued

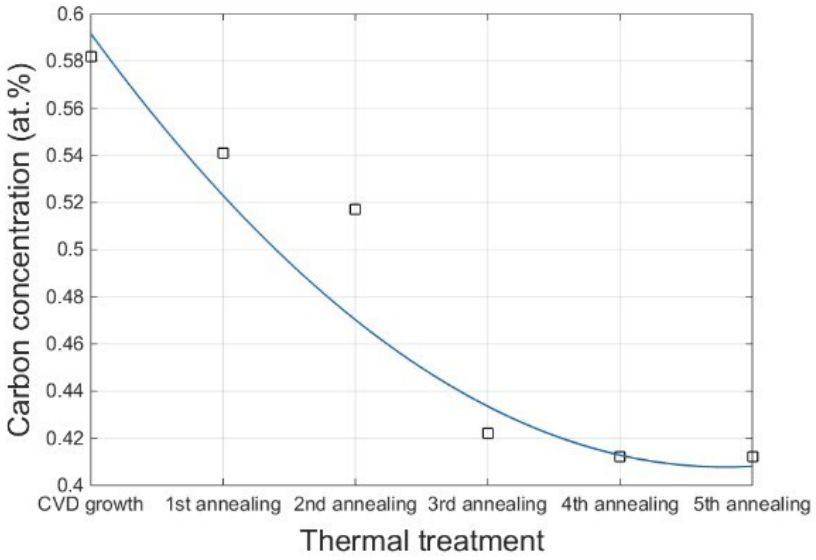


Figure 4.7: SIMS data from the growth foil after each of the consecutive annealing steps plotted together with a trend line.

at 0.41 at%. This could be related to the carbon depletion effect that was observed when the process became unable to form complete graphene layers. By calculation, carbon solubility in the Ni/Cu foil can be determined. Cu and Ni have a solubility of 0.00045 at% [162] and 0.9 at% [163] respectively. This means that the 55/45 Cu/Ni foils should have a carbon solubility of about $(0.00045 \cdot 0.55 + 0.9 \cdot 0.45) = 0.405 at\%$. Therefore, the concentration of carbon CVD growth indicates a supersaturation of the foil which made it possible to extract graphene down to a concentration of about 0.41 at%, which is close to the theoretical value.

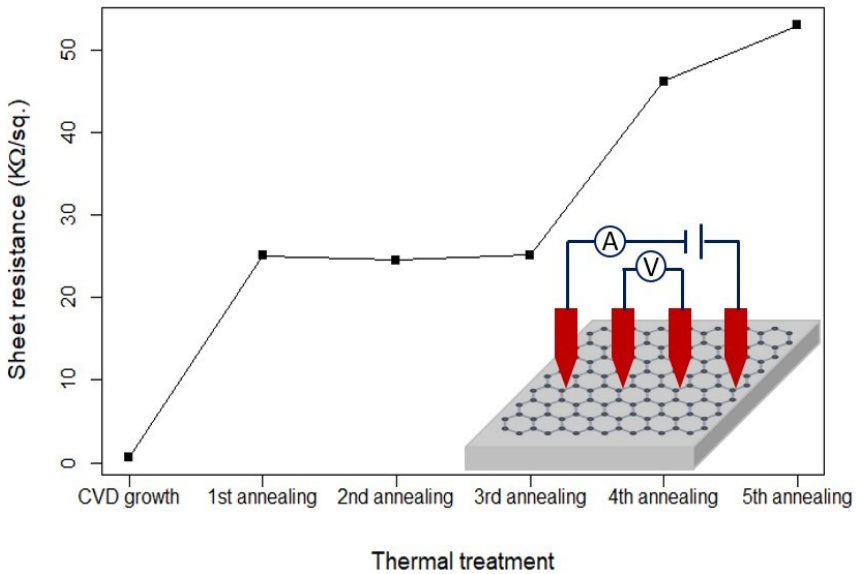


Figure 4.8: 4-point probe measurement of the electrical sheet resistance of the grown graphene at every growth step.

Finally, the produced graphene films were evaluated using the 4-point probe measurement on the Si/SiO_2 chips for determination of the sheet resistance and the results are presented in Figure 4.8. As seen, the sheet resistance of the first CVD grown graphite film is measured to 0.6 k$\Omega/\square$. This value then increases up to and stabilizes at a value of 25 k$\Omega/\square$ for the 1st, 2nd and 3rd annealing samples. This indicates that the quality is consistent in between these three annealing cycles, which previously concluded through Raman scans presented in Figure 4.4 and 4.5. The sheet resistance then increases for both the 4th and 5th annealing cycles up to a final value of 53 k$\Omega/\square$.

This novel technique of repeated graphene growth on foils after one single carbon saturation shows promise for convenient graphene fabrication. The growth was shown to be stable up to three consecutive annealing cycles which each would generate 1 - 3 layers of graphene. Further improvements to this growth method will be possible by tuning the foil composition resulting in an increased carbon solubility with improved growth control. By increasing the as-grown and as-transferred graphene crystallinity, lower sheet resistances should be attainable for horizontal VLSI interconnects.

4.2 Cu/CNT Composite TSV for 3D Packaging Applications

A future replacement of Cu based TSVs should have high current carrying capacity (ampacity) at the same time as it should demonstrate high conductivity (reciprocal resistivity). These two properties are traditionally seen as mutually exclusive as conductivity and ampacity are associated with tightly and loosely bonded electron structures, respectively [164]. Therefore, by combining Cu (tightly bonded electron structure) and CNTs (loosely bonded electron structure), a composite can be fabricated that combines both of these properties. This has previously been demonstrated with an improvement of two order of magnitude in ampacity without reducing the conductivity compared to Cu. This composite also demonstrates a reduced skin effect [165] and modelling shows that the material exhibits lower signal delays in respect to interconnect length than both Cu and CNT individually [166]. Additionally, the Cu/CNT composite can be combined with an epoxy liner in the via. This results in a CTE mismatch to Si that is drastically reduced and enables large improvements in terms of reliability [167]. All of these factors make the Cu/CNT composite TSV an ideal contender for replacing traditional Cu TSVs for the next generation of 3D IC packages.

A 3D package designed around co-planar waveguides (CPW) transmission lines was fabricated and assembled with the intention to measure the RF properties of the Cu/CNT TSV structures. An illustration of the package is found in Figure 4.9.

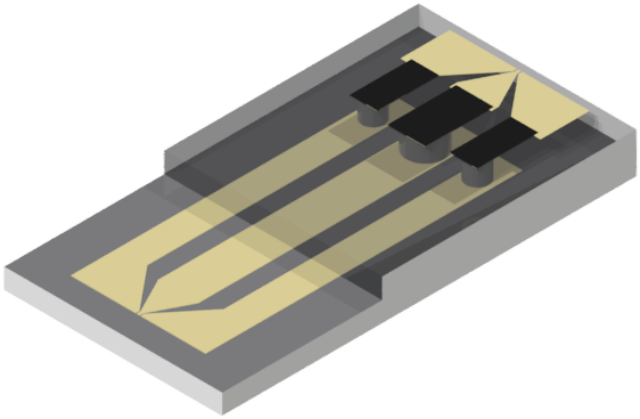


Figure 4.9: 3D package fabricated to test RF performance of the Cu/CNT TSVs using Au CPW transmission lines. A Si chip populated with TSVs is connected to a carrier chip patterned with Au CPW transmission lines.

The fabrication process of the Cu/CNT bundles is presented in Figure 4.10 and is based on ordinary CVD growth of vertically alligned CNT arrays which previously been covered in Chapter 2.1. The CNT bundle design needs to fulfill a number of criteria to result in high performing TSVs: CNT bundles needs to be grown with maintained structure integrity in a length corresponding to the Si via it is supposed to populate. The bundle also needs to provide enough space for the ions in the plating solution in order to facilitate a proper coverage of the entire surface of the bundle. Therefore, to properly fabricate a Cu/CNT composite of the CNT array, some thought had to go into the patterning in order to allow Cu to fully infiltrate the array. This was done by a design based on the work by Sun et al. [167] that separated the CNTs into small bundles with a diameter of 20 µm. However, growth of CNTs using this pattern proved problematic as the bundles were too small and separated to provide support for each other. This resulted in collapse of the CNT structure during growth which rendered the CNT bundles impractical for further use in the process. To solve this issue, a support ring was added to the design which helped the bundles maintain its form and structure. The final pattern with the added support ring is presented Figure 4.10A and an SEM image of the as-grown CNT bundle is shown in Figure 4.10B. This structure was sputtered with an electrically conducting layer of Ti/Au to prepare the bundles for Cu plating, seen in Figure 4.10C. Two issues arose in the electroplating step. First, the prepared CNT design was proved not to allow a satisfactory penetration into the CNT bundle structure and would leave most of the plated Cu on the tip and side walls of the bundle. This can be seen in the SEM image in Figure 4.10D that shows that the Cu have not been able to grow in-between the smaller 20 µm CNT structures. This means that Cu loading is reduced and that a longer plating time is necessary to obtain a decent conductivity in the resulting TSV structure. The second issue is a direct result of the increased plating time. The amount of Cu on the support ring effectively welded the CNT bundles to the growth substrate and thereby obstructed a transfer over to the via substrate in the later steps of the process.

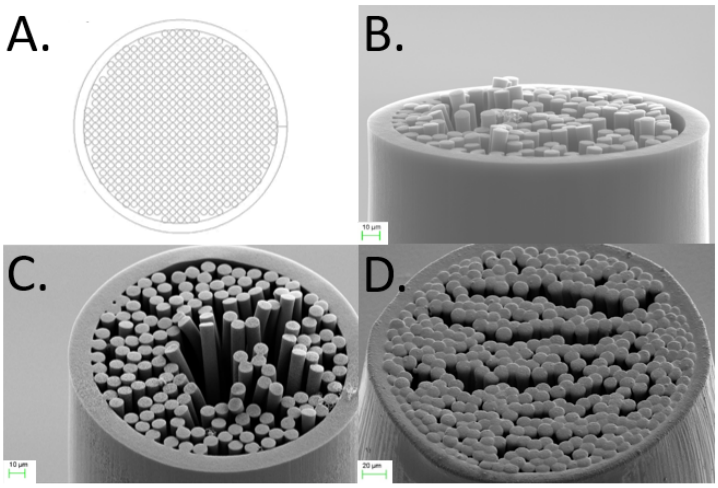


Figure 4.10: Different steps in the Cu/CNT fabrication process: A) Design of the CNT catalyst pattern. B) Top side view of the as-grown CNT array bundle. C) CNT bundle after Ti/Au sputtering. D) Final result of the Cu/CNT composite bundle.

The fabrication of the via chip was conducted using standard CMOS processes and is illustrated in Figure 4.11. This process utilized a deep reactive ion etching (DRIE) step to form the high aspect ratio via holes through the Si wafer. A patterned Al hard mask was used on top of the Si wafer in the DIRE process as it provides a much higher selectivity than photoresist masks. The Al hard mask was removed after DRIE in an Al etch bath and the Si wafer was subsequently cleaned using the RCA cleaning procedure [168]. Finally, a 100 nm thick thermal oxide dielectric was grown on the entire Si wafer including the inner walls of the vias.

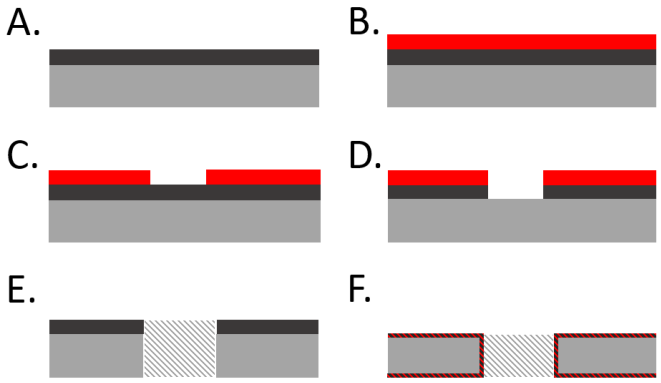


Figure 4.11: Fabrication process steps to prepare Si chips with SiO_2 passivated vias: A) Al hard mask sputtering. B) Photoresist deposition. C) Exposure and development of photoresist. D) Al-etch to transfer photoresist pattern to the Al hard mask. E) DRIE processing to transfer the Al hard mask pattern down into the Si and thus forming via holes. F) Removal of Al hard mask, RCA clean and thermal oxide growth on the Si.

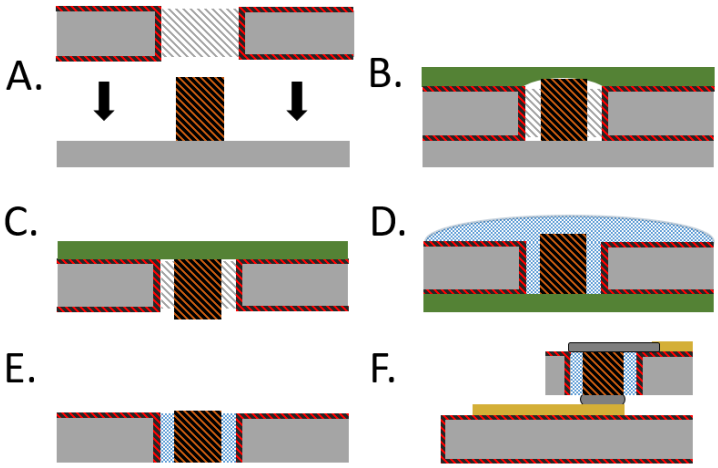


Figure 4.12: Cu/CNT TSV transfer processs: A) Via chip is aligned with Cu/CNT bundles. B) Kapton tape is placed on the Si surface in contact with the Cu/CNT bundle tips. C) CNT growth substrate is removed by shearing. D) Epoxy solution is vacuum infiltrated into the via holes and cured. E) Si substrate is CMP lapped on the epoxy-side down to the Si surface and the tape is removed. F) Si chip is patterned with contacts and integrated into a CPW 3D package.

Via chips were diced from the wafer and used to transfer the Cu/CNT bundles as illustrated in Figure 4.12. This was done using the tape assisted transfer method by Mu et al. [169]. The Cu/CNT bundles was placed in the via holes on the Si chip by alignment by hand before a tape was placed on top of the chip and pressed in contact with the Cu/CNT bundles. The Cu/CNT bundle transfer required some shearing force before the bundles would release from the growth substrate. Once transferred, a two component self curing epoxy was used to vacuum infiltrate the vias with the intention that it would fill the purpose as an epoxy liner. The liner is important as it is supposed to provide mechanical support and act as a dielectric barrier. The tape efficiently protected the surface it was attached to during planarization using chemical mechanical polishing (CMP) and remaining adhesive residues was removed with cotton tips soaked in IPA/acetone. Choice of tape for the transfer process proved to be of importance and two different types were tested, ordinary kapton tape and red thermal release tape (rated up to 170°C). The stiffness of the thermal release tape resulted in TSVs that were partially covered by epoxy after tape removal, as seen in Figure 4.13A. Oxygen plasma removal of this extra epoxy layer on top of the TSV proved to be difficult and the issue was solved by using the more flexible kapton tape for the transfer instead. Photoresist remover incompatibility was another issue that appeared during the later steps in the process while patterning the TSV chips with Au contacts for the CPW transmission lines. The epoxy liner in the vias proved to be dissolved by the remover (NMP based) which in turn destroyed the TSV structure as a result as seen in Figure 4.13B.

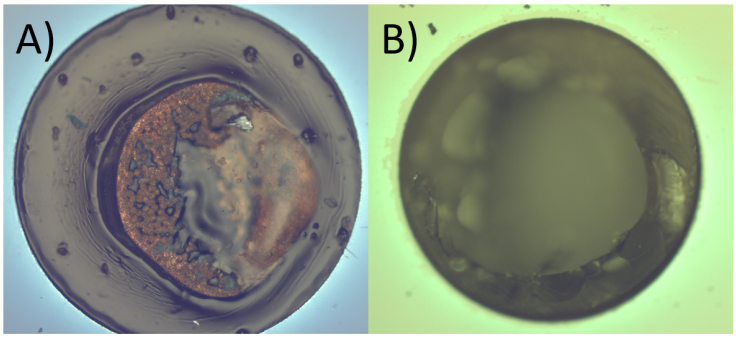


Figure 4.13: Microscope photos showing vias on the Si chip: A) Before submersion in photoresist remover. B) After remover bath which resulted in TSV failure.

Several types of removers were tested including pure solvents like acetone and they all resulted in TSV failure. One sample did survive the final processing step and was integrated into the final 3D package as intended using a isotropic conductive adhesive (ICA) filled with graphene flakes. The ideal when it comes to RF performance is to use purly ohmic contacts (solder) instead of capacitive ones that arises in electrical contacts based on ICA (or its anisotropic counterpart, ACA). However, the many process limitations found during the fabrication forced the use of ICA to finalize the package.

One chip housing several Cu/CNT TSVs was singled out before the final patterning steps in the proceess for measurement of the resistance and resistivity of the Cu/CNT bundles through 4-point probe measurement. This was possible after shortcircuting all the TSVs from the backside of the Si chip through Ti/Au sputtering. The results are presented in Figure 4.14.

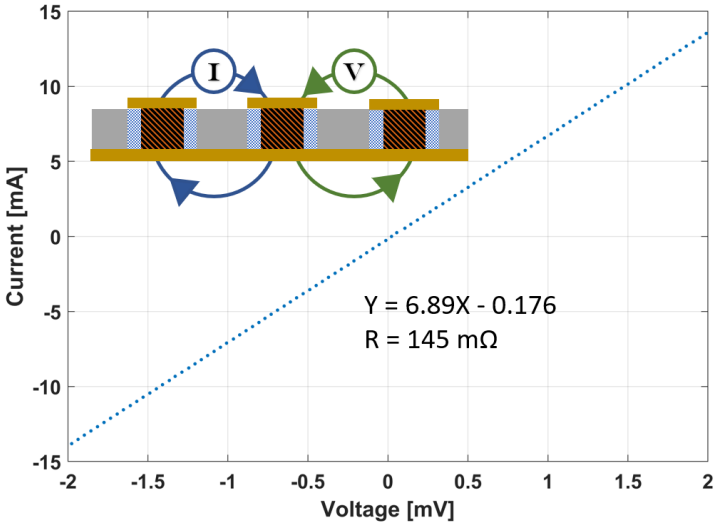


Figure 4.14: IV curve from 4 point probe measurement of the Cu/CNT TSVs. Inset depicts the 4 point probe configuration used to single out the resistance contribution of a single TSV.

The resistance measurement was performed by a sweep from -15 mA to 15 mA. The measured resistance over this range was found to be R = 145mΩ after slope fitting. The resistivity can be found using the TSV dimensions and is caluculated by the equation:

$$Resistivity = \frac{TSV area \cdot Resistance}{TSV length} \tag{4.1}$$

In this case, the TSV depth was 280 µm and the TSV diameter was 300 µm. This gives a resistivity of $3.66 \cdot 10^{-5} \Omega m$. These results are interesting since the value is about 90 times larger then previous results [167]. This can be explained as a consequence of the transfer issues found related to the Cu loading. Improved resistivity values will therefore be attainable by tuning the pattern to allow for an even Cu coating of the entire CNT bundle while still retaining their transferability.

The RF performance of the CPW transmission line package was evaluated using S-parameter test measurements. Signal losses originated from the TSV structures could be singled out by first measuring 2D Au CPW tranmission lines and comparing these results to the 3D Cu/CNT TSV package. The RF performance was measured using a two port s-parameter test in the 1 - 10 GHz range. The results are presented in Figure 4.15.

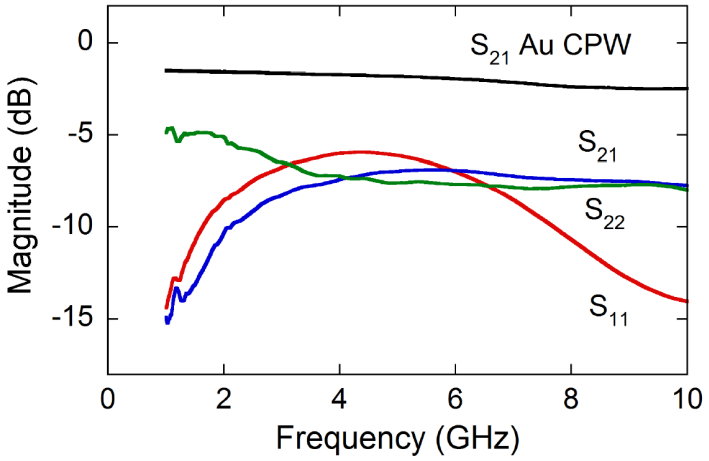


Figure 4.15: S-parameters: S21 (blue), S11 (red, contacts on the carrier substrate) and S22 (green, contacts on the top chip) for the Cu/CNT TSV CPW structure as well as S21 (black) for the Au reference CPW structure.

The S-parameters demonstrate an immediate increase in signal loss S21 = -5.5 dB associated with the addition of the Cu/CNT TSV structures. This increase in signal loss might either originate from the TSV itself or the graphene ICA used to connect it to the carrier chip. Additionally, capacitive losses are demonstrated for S21 and S11 which should be a direct consequence of the ICA used to connect the TSV chip to the carrier. However, previous research on CNT based TSV structures have reported S21 results at 10 GHz ranging from -0.9 up to -10 dB when measuring

the RF signal losses [170, 171]. These results can be compared with the signal loss performance of pure Cu TSVs with SiO_2 dielectric liners that yielded -0.75 dB over two TSVs in series [172]. Furthermore, similar capacitive contact effects have been found in CNT based TSVs which indicates that a proper loading of Cu might solve this issue [173].

Many of the encountered issues during the fabrication and measurement of the Cu/CNT TSVs were related to the CNT pattern or the epoxy liner. A new CNT pattern is required which should focus on maximizing bundle surface area available for plating without sacrificing the structural integrity. Such a CNT pattern could serve as the foundation for Cu/CNT TSVs that are easy to transfer while still providing high conductivity. A new epoxy liner is also required in order to allow CMOS processing on the chip after the TSV structures are formed. This, in turn, would allow fabrication of a proper solder mask and under bump metallization that will allow flip chip integration. This way solder bumps can be used to connect the 3D package which would reduce the RF signal losses and remove the previously observed capacitive effects.

4.3 Conclusions

Two different types of low dimensional carbon nanomaterials were explored for interconnect applications. Horizontal and vertical interconnects based on graphene and vertically grown CNTs have been developed and fabricated by exploiting the structure of these materials.

First, a novel production approach is discussed that can enable a growth foil to store large amounts of disassociated carbon available for multiple synthesis cycles of graphene. This way, foils could be pre-saturated and distributed before the graphene synthesis and transfer which could make the material handling more practical. However, engineering of the foil composition is still required to ensure the quality and increase the number of growth cycles available. Further development should include precise tuning of the catalyst composition deposited onto a scaffold. This way, interconnect geometries could be pre-templated in precise geometries (like nano ribbons etc) on the scaffold and in turn directly transferred to the intended circuit.

The second application was a Cu/CNT composite designed for TSV interconnects. The Cu/CNT composite has been demonstrated as advantageous in terms of performance and reliability. However, fabrication revealed that further work is required on both CNT patterning as well as chip integration. These restrictions should, however, be possible to remove by a redesign of the CNT pattern to improve the Cu loading and by changing the epoxy liner effectively making the process CMOS compatible.

These two studies find that low dimensional carbon nanomaterials indeed are promising as future 'non-Cu' interconnect materials for VLSI applications. However, carbon nanomaterials are disruptive technologies that will require new processes and methods to properly integrate them into CMOS production flows.

Chapter 5

Annealing of Carbon Nanotube Arrays through High Temperature Heat Treatment

Much of the academic and industrial focus on graphene and CNTs comes from their exceptionally high bulk electrical and thermal conductivity that have been reported in literature [174, 175]. Unfortunately, the reported performance of graphene and CNTs is often based on theoretical calculations and measurements under ideal conditions which can be difficult to realize without a complete mastery of the material. The reality is that the effective electrical and thermal conduction properties of these materials are not only dependent on the bulk conductivity but also on the contact resistances on either side of the material [176, 177]. Much of Chapter 2 in this thesis already discusses strategies on how to minimize the contact resistance to the mating substrate of CNT array TIMs by different bonding methods. Therefore, this chapter will focus on how to improve the material itself and follow the work published in Paper H.

5.1 High temperature annealing of CNT arrays

Vertically aligned CNTs are interesting for both thermal management and electrical interconnect applications. The reason for this is the highly aligned nanowire structure that allows direct conduction in one dimension between the two points that the CNT is fixated between. This means that both the effective electrical and thermal transfer over the CNT can be described as the sum of the resistance in the two contacts and the CNT length divided by its bulk conductivity (Equation 1.3). In the case of CVD grown CNTs there are mainly three bottlenecks present already after growth: catalyst under-layers, defects and density. The catalyst under-layers results in a contact resistance contribution that limits thermal conduction and isolates electrical conduction [98]. The large concentration of defects in the CNT lattice limits thermal, electrical and mechanical properties of the individual tubes [178]. Finally, the low

density of CNTs present in the array means that there are few individual tubes that can contribute the the array overall properties [179].

The thermal conductivity of isolated individual CVD grown CNTs has been demonstrated to only reach 600 W/mK [180] which is about 20 % of the thermal conductivity CNTs have been demonstrated to possess otherwise [175]. This limitation is directly tied to the crystallinity ratio ($\frac{I_D}{I_G}$ from Raman spectroscopy). Furthermore, the effective thermal conductivity of CNTs in an array will be even lower due to the low density that can be expected from CVD grown CNTs and have been measured to only 70 W/mK in our own experiments [49]. This issue has already been the focus of many publications in literature and methods for high density growths have been demonstrated being possible using standard micro fabrication techniques [179]. At the same time, it is not obvious that an increased CNT array density would be beneficial due to drawbacks in terms of mechanical complacency that might hinder effective contacts being formed during interface closing [181].

The bulk crystallinity of CNTs can be measured using Raman spectroscopy [182]. The crystallinity ratio of our CVD grown CNT arrays was found to be > 1.2 according to Figure 2.25, which can be compared to graphene that lost $\approx 80\%$ of its thermal conductivity as the crystallinity ratio increased from 0.13 - 1.00 [182]. One way of increasing the crystallinity and removing defects in carbon nanomaterials is by high temperature treatment at temperatures above 2850°C [183]. This effect has previously been demonstrated for both graphene-based films [120] and individual CNTs [183] followed by a subsequent growth of crystallites within the film/walls [184]. However, since CNT arrays normally are grown on substrates with relatively low melting temperatures like Si (1414°C), this method for quality enhancement becomes difficult to utilize without transferring the as-grown CNT array structure. This issue was solved by the development of the graphene CNT hybrid structure that used a graphitic film as-growth substrate for CVD synthesis of CNT arrays which was discussed in Chapter 2.3.3. This way, high temperature treatment of CNT arrays could be achieved in order to anneal the CNT lattice without altering the as grown array structure.

There are two main ways of growing CNT arrays using CVD methods [68]. The first and most usual way is called the base-growth approach which results in CNTs growing up from the catalyst particle resulting in an array that is connected to the growth substrate through the catalyst stack. The other approach switches the layers in the stack and results in a tip-growth with the catalyst stack on the top side of the array. This means that in either case there is a residual catalyst stack, on top in the case of tip-growth and in between the substrate and the array in the case of base-growth. As a consequence the thermal and electrical conduction through the array will be restricted [185]. However, as the growth quality of the bottom up approach is superior this is also the method of choice for most applications even though the catalyst stack becomes built in to the material and therefore difficult to deal with. However, both Fe and Al_2O_3 should have an evaporation temperature

below 3000°C which in principle would remove the catalyst stack from the array. Furthermore, if the used growth substrate is graphicic in nature, this could result in the CNTs fusing into the growth substrate and that way reducing the contact resistance.

Samples for the high temperature annealing of CNT arrays were prepared by 'bottom up' CVD growth on PGS films. The growth substrates were prepared by deposition of a normal catalyst stack consisting of 10/1 nm Al_2O_3/Fe on PGS films using e-beam evaporation. The substrates were then used to grow CNTs using the modified joule self heating method described in Chapter 2.3.3.

5.2 Annealing Effect on Crystalline Structure

To evaluate the effects of heat treatment on CNT arrays grown on PGS substrates, measurements before and after treatment were made. These measurements were conducted using Raman spectroscopy, XPS and TEM as the main focus of the study was on the crystallinity and the catalyst stack in between the CNT and the PGS. Results from the Raman spectroscopy measurements are presented in Figure 5.1.

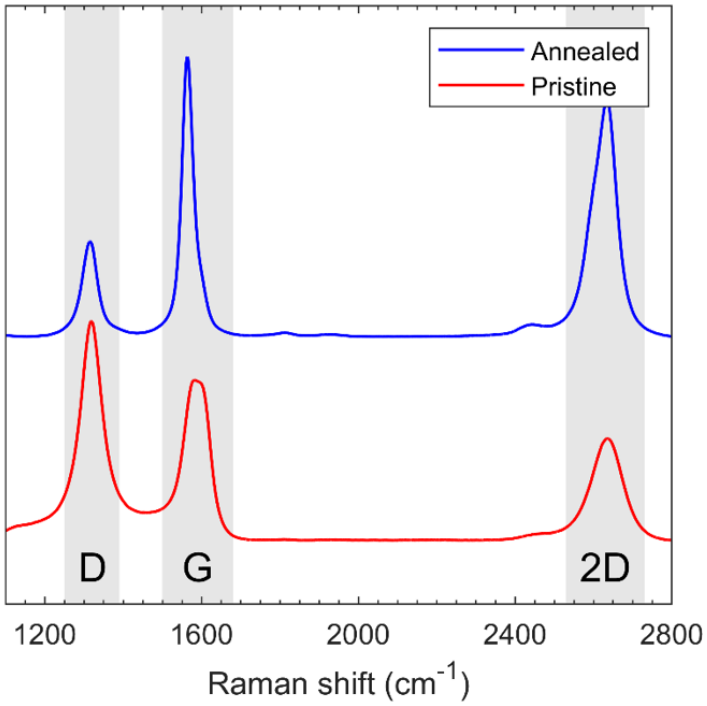


Figure 5.1: Spectroscopic data from Raman measurement of CNTs before (pristine) and after (annealed) heat treatment.

As seen, the CNT arrays before treatment display a similar defect concentration to earlier Raman studies on CNT arrays (Figure 2.25) with a $\frac{I_D}{I_G}$ peak ratio of > 1.3. In contrast, the samples after heat treatment display a decreased $\frac{I_D}{I_G}$ peak ratio to ≈ 0.35 which is a strong indication of decreased defect density [186]. Furthermore, the spectrum associated with the annealed sample shows more pronounced G and 2D peaks with are associated with a higher degree of graphitisation in the tubes [187]. These results show an obvious decrease in defect concentration within the CNT lattice. To further analyze the heat treatment effect of the defect concentration as well as wall counts TEM was used to image the CNT before and after treatment. The TEM images are presented in Figure 5.2

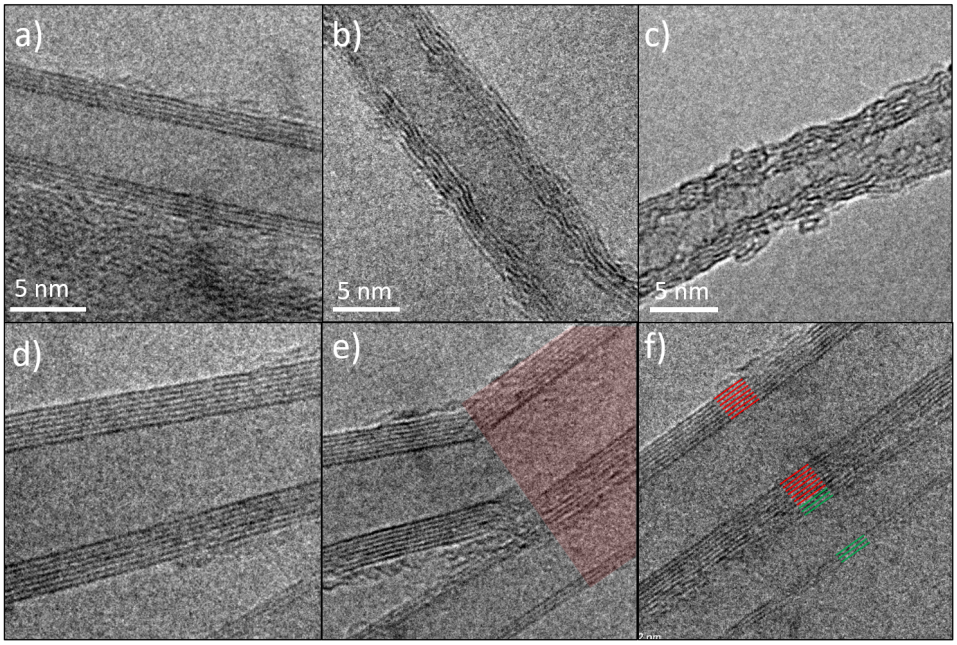


Figure 5.2: Effects of heat treatment is visualized through TEM images. a) The straight wall structure of an annealed CNT. b) Pristine CNT obtained through CVD growth with wavy walls. c) Irregularities and defects along the walls of a pristine CNT. d) - f) Heat treatment makes the CNT strands straighten out and grow together.

The CNTs are imaged using TEM to illustrate the changes before and after heat treatment by imaging the crystalline structure of the CNTs. Figure 5.2 a) presents an annealed CNT strand with its straight and well defined structure. This appearance can be directly compared with that of the pristine CNT strand in Figure 5.2 b) and c). In comparison, the pristine CNT shows a less defined structure and is even found with smaller chunks of amorphous carbon along the wall structure, features both linked to the crystallinity of the CNT. Defects in the CNT lattice make room for irregular bends and uneven angles that a perfect crystal would not. Also, lattice irregularities, uneven charge distribution and dangling bonds will attract and keep foreign objects and elements physisorbed along the CNT wall structure. Therefore, an annealing process will straighten out the wall structure of the CNT. Another

interesting effect is imaged in Figure 5.2 d) to f) that show how two CNT have grown together and formed a structure with larger amount of walls in-between them.

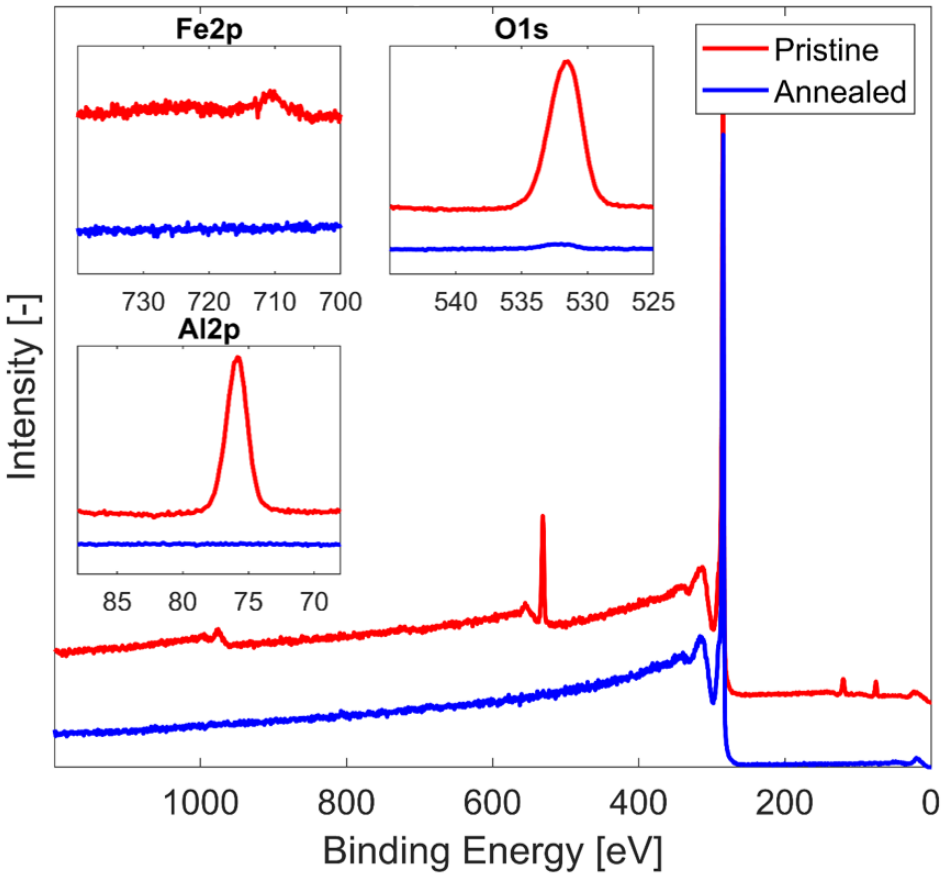


Figure 5.3: Chemical comparison of the CNT before and after annealing through XPS scans. Insets show multiplex scans of Fe2p, O1s and Al2p peaks.

Further chemical analysis of the samples before and after treatment was conducted using XPS and can be found in Figure 5.3 in which both full acquisitions as well as multiplex scans of the main elements Al, O and Fe are presented. The presence of Al, Fe and O is directly linked to the catalyst under-layers that consist of Al_2O_3 and Fe. However, the large peak associated with O is also connected to oxygen contamination that always shows up together with adventitious carbon after exposing samples to ambience. The XPS results show a complete removal of Fe and Al and a drastic decrease in the O peak after heat treatment. This indicates that the catalyst under-layers are evaporated during heat treatment and that the structure of the CNTs somehow have fused together with the PGS substrate underneath as the array still retains its vertical orientation. Further investigation on the exact nature of this remains to be investigated. However, previous reports have concluded that CNTs can grow into a graphene layer to form a continuous sp^2 structure [185].

The structural and chemical analysis of the CNTs show a drastic decrease of defects after heat treatment. This process both straightens out the tube structure, heals the lattice structure and fuses walls from different CNTs together. Additionally, chemical analysis shows that the catalyst under-layers are gone after heat treatment which indicates an evaporation of the Al_2O_3 and Fe that normally resides there. This implies that heat treatment of CNT arrays on graphite substrates can increase the thermal and electrical bulk conductivities of the structure as well as remove the interface resistance that otherwise resides in the catalyst anchoring point in-between substrate and array.

5.3 Array Densification

A side effect of the heat treatment on CNT arrays was a densification similar to that achieved using capillary driven densification [83, 188]. This resulted in the array deforming into highly densified bundles instead of keeping the normal forest-like array structure. This effect was studied by subjecting CNT arrays to different temperatures and evaluating the densification. This was done in two steps, 1000°C, 1200°C which in turn was compared to the results from the 3000°C heat treatment. These temperature steps were chosen as the ovens the we had available only could reach up to 1200°C and that we could start to see an effect already at 1000°C. The results are presented in Figure 5.4.

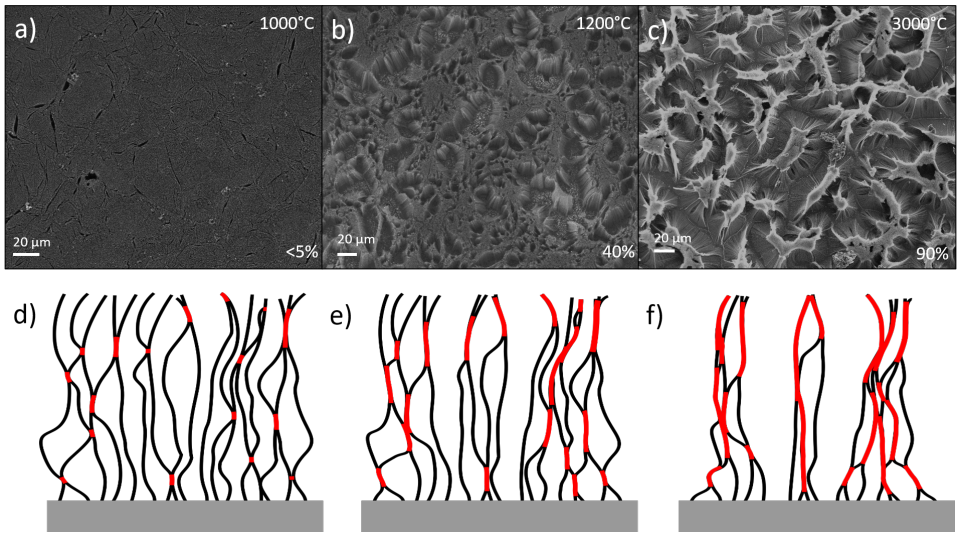


Figure 5.4: Figure a) - c): SEM images of the arrays after 1000°C, 1200°C and 3000°C respectively. Figure d) - f): Illustration of how the annealing process gradually draws the CNT strands closer together.

The densification effect was quantified by measurement of the relative tips area. This was done using image analysis software (ImageJ) on SEM images taken on the surface of the samples. These results showed that samples annealed at 1000°C had densified less than 5 %. The samples heat treated at 1200°C had a considerably higher

densification which revealed about 40 % of the underlying surface. Finally, samples heat treated at 3000°C had reached a densification of > 90 %. These results fall in line with the decomposition temperature for many of the C-O functional groups that are present in the CNT wall structure after growth. This is confirmed further by the decrease in oxygen content from the XPS measurements presented in Figure 5.3. By removing these oxygen containing groups that provide electrostatic repulsion between the CNTs in the array, van der Waals attraction can dominate and densification is allowed to occur. Once the CNT walls come into contact with each other they start to merge and densify into compact bundles which drives the densification further.

5.4 Conclusion

The study of heat treatment effects on CNT arrays grown on graphite substrates has been conducted using Raman spectroscopy, XPS, TEM and SEM. These measurements demonstrate that heat treatment at 3000°C causes the CNT to heal the graphene walls and thereby improves the crystallinity. A side effect of the crystallite growth is that the CNTs straightens themselves out and walls in contact with each other grow together. As the increased crystallinity will be directly linked to the mechanical, thermal and electrical properties of the CNT this show promise for future CNT application where CVD grown CNTs traditionally has been lacking.

The densification side effect during heat treatment is normally restricting the potential use for CNTs in many applications where an intact array is desirable. However, published literature has previously demonstrated the use of vapour densification for CNT based TSVs where a CNT array is grown with larger footprint than necessary and then shrunken into the correct dimensions before transfer [189]. By densification using our method instead, a simultaneous densification and quality improvement can be achieved resulting in far better performance. Additionally, this research opens up new interconnect design possibilities due to the demonstrated elimination of catalyst under-layers.

Chapter 6

Future Directions

This thesis outlines my work on carbon nanomaterials for electronic packaging applications. While the provided designs already show promise as capable successors for established industry standards, there are still much potential to unlock. Here are some of my ideas on how to continue the research and speed up the industry adoption of carbon nanomaterials for thermal management and interconnect applications in micro electronic devices.

- **Improved thermal dissipation of CNT array TIMs** – State-of-the-art CNT array TIMs already show excellent performance in terms of bulk thermal resistance. However, this thesis finds that the array length of CNT array TIMs needs to be increased in order to improve the reliability. Unfortunately, this will affect the performance, making the CNT bulk resistance a bottleneck that limits the thermal dissipation. To compensate for the increased CNT length, CNT arrays should be grown with an increased density which will improve the effective thermal conductivity of the array. An increased array density might also obstruct the conformability of the array and will thus require improved bonding solutions to compensate.

- **General design guide for CNT array TIM systems** — The reliability work presented in this thesis resulted in a model to describe the relation between thermal resistance degradation and CNT array length. However, this model needs to be developed further with empirical data taking effects like lateral substrate size, CTE mismatch and CNT crystallinity into account. Furthermore, CNT array TIM systems without catalyst under-layers (transferred and double bonded) needs to be challenged to assess their reliability constraints.

- **Controlled release of catalyst particles** — One fundamental issue with CNT array TIMs resides in the CMOS incompatibility of the growth process. This limits the use of CNT arrays in TIM applications and requires transfer to the active chip, which skews and distorts the array in the process. One of the findings in this thesis is an oxidative effect on the iron catalyst particle that might facilitate an efficient release of the CNTs from the growth substrate.

This effect could in turn be exploited for efficient transfer of arrays regardless of application.

- **Joule annealing of carbon nanomaterials** — This thesis concludes that the performance of CNT arrays is severely limited by the high defect concentration that is inherent from the CVD process. This can be countered by high temperature annealing which has been shown to heal the crystal lattice of the CNTs and improve the overall structure. However, the temperatures required to reach this effect is too high for conventional ovens which makes it unpractical for further research. Therefore, the joule heating effect in vacuum might be a convenient way to reach the necessary temperatures and should allow further development of these materials without the large investment costs otherwise associated with carbon annealing. This way, an improved crystallinity and efficient removal of catalyst particles will improve electrical, thermal and mechanical properties of the system.

- **Graphene/CNT hybrid 3D interconnect systems** — The work on electrical interconnects covered in this thesis dealt with graphene grown as horizontal transmission lines as well as CNT bundles intended for vertical TSVs. By combining this work with the graphene-based film CNT hybrid structure that was developed in this thesis, a new material design for 3D VLSI interconnects can be achieved. This material could serve as a basis for interconnects by patterning CNT TSVs on graphene films and integrating it into via chips. Once in place, the graphene film would be etched into transmission lines of the desired shape before stacking multiple layers of such chips into a complete 3D system.

Chapter 7

Summary of Papers

Paper A

Current status and progress of organic functionalization of CNT based thermal interface materials for electronics cooling applications
Andreas Nylander, Yifeng Fu, Lilei Ye, and Johan Liu. *Proceedings of IMAPS Nordic Conference on Microelectronics Packaging (NordPac)*, 2017

This paper takes a closer look at organic functionalization methods for carbon nanotube thermal interface materials in literature. All the data is summarized and observed trends are outlined.

My contribution: Data collection, analysis, interpretation and paper writing.

Paper B

Covalent anchoring of carbon nanotube-based thermal interface materials using epoxy-silane monolayers
Andreas Nylander, Yifeng Fu, Mingliang Huang, and Johan Liu. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 9, no. 3 (2018): 427-433.

This paper presents a novel functionalization approach for carbon nanotube thermal interface materials based on epoxy-silane self-assembly chemistry. The interface structure consists of a monolayer functionalized silicon chip and a carbon nanotube array prepared by nitrogen plasma bonded by epoxy chemistry. Characterization is performed by ellipsometry, AFM, XPS and the thermal interfaces are evaluated by the flash method for assessment of their thermal interface resistance.

My contribution: Experimental design, sample fabrication, characterization and paper writing.

Paper C

Reliability investigation of a carbon nanotube array thermal Interface material
Andreas Nylander, Josef Hansson, Majid Kabiri Samani, Christian Chandra Darmawan, Ana Borta Boyon, Laurent Divay, Lilei Ye, Yifeng Fu, Afshin Ziaei, and Johan Liu. *Energies* 12, no. 11 (2019): 2080.

This paper investigates reliability aspects for a carbon nanotube array thermal interface based on a HLK5 polymer bonding functionalization. The samples are subjected to accelerated aging through thermal cycling and analysed for its thermal interface resistance degradation using the flash method. Failure analysis reveal that the interfaces fail on the nanotube root side and XPS characterization shows that the bonding between the nanotube and the growth substrate is weakened by oxidation. This study concludes that the reliability of carbon nanotube array interfaces needs further research before the technology can mature.

My contribution: Concept development, experiment, paper writing together with Josef Hansson.

Paper D

Synthesis of a Graphene Carbon Nanotube Hybrid Film by Joule Self-Heating CVD for Thermal Applications
Josef Hansson, Majid Kabiri Samani, **Andreas Nylander**, Lilei Ye, Nan Wang, Torbjörn Nilsson, and Johan Liu. *Proceedings of IEEE 68th Electronic Components and Technology Conference (ECTC)*, pp. 2450-2456. IEEE, 2018.

This paper uses a novel CVD joule self-heating method to grow double bonded CNT on graphene-based film interposer structure. Pre-patterned graphene-based films are heated inside a CVD chamber for growth directly on the film, thus eliminating temperature offset issues that will reduce the quality of double side bonded structures. The material is characterized for its array alignment, thermal properties and defects. The final interposer is applied as a thermal interface material and is shown to outperform similar commercially available solutions.

My contribution: Chemical and thermal characterization of the material.

Paper E

Degradation of Carbon Nanotube Array Thermal Interface Materials Through Thermal Aging: Effects of Bonding, Array Height and Catalyst Oxidation
Andreas Nylander*, Josef Hansson*, Torbjörn Nilsson, Lilei Ye, Yifeng Fu, Johan Liu. *Submitted to Applied materials and interfaces*

This paper presents a systematic study as a continuation on Paper III on the reliability of carbon nanotube array thermal interface materials. The failure mechanisms are explored further by investigating length dependence, CTE mismatch and chemical degradation issues. The paper provides a design guide for reliable carbon nanotube thermal interface materials.

My contribution: Josef Hansson and I designed the concept, designed the experiments, fabricated the samples and performed the testing and characterization as well as wrote the paper together.

Paper F

Multiple growth of graphene from a pre-dissolved carbon source
Andrea Fazi*, **Andreas Nylander***, Abdelhafid Zehri, Jie Sun, Per Malmberg, Lilei Ye, Johan Liu, and Yifeng Fu. *Nanotechnology*, 31, no. 34 (2020): 345601.

This paper explores a CVD synthesis method for graphene. By saturating a NiCu foil with carbon in a CVD chamber, we show that it is possible to achieve multiple subsequent growths of graphene from the same foil without the presence of carbon precursors. The resulting graphene is characterized by Raman mappings, TEM and 4-point probe electrical measurement to verify the quality of the as grown graphene. Furthermore, SIMS is used to analyze the concentration of carbon content in the foil after each subsequent growth until depletion.

My contribution: Chemical characterization as well as paper writing.

Paper G

RF Properties of Carbon Nanotube/Copper Composite Through Silicon Via Based CPW Structure for 3D Integrated Circuits
Andreas Nylander, Marlene Bonmann, Andrei Vorobiev, Josef Hansson, Nan Wang, Yifeng Fu, and Johan Liu. *Proceedings of IEEE 14th Nanotechnology Materials and Devices Conference (NMDC)*, pp. 1-5. IEEE, 2019.

This paper demonstrates the use of carbon nanotube/Cu composite structures as through silicon vias for 3D integrated IC applications. The fabrication process is outlined, and the resulting structures are integrated into silicon chips as vertical interconnects. Characterization is performed by 4-point probe measurements as well as S-parameter test.

My contribution: Concept development, sample fabrication, measurement together with Marlene Bonmann and paper writing.

Paper H

Effects of high temperature treatment of carbon nanotube arrays on graphite: increased crystallinity, anchoring and inter-tube bonding
Josef Hansson, **Andreas Nylander**, Mattias Flygare, Krister Svensson, Lilei Ye, Torbjörn MJ Nilsson, Yifeng Fu, and Johan Liu. *Nanotechnology*, 2020.

This paper presents a high temperature treatment method for carbon nanotube arrays. Annealing is performed by subjecting carbon nanotube arrays grown on graphite substrates by the method in Paper IV to temperatures as high as 3000°C. The annealing is shown by Raman and XPS analysis to increase the crystallinity of the nanotubes as well as eliminate the catalyst under-layers present in the structure. TEM analysis show a straightening effect of the carbon nanotubes, which is believed to occur as a consequence of the reduced amount of defects present. Furthermore, adjacent nanotubes are observed to fuse together with a graphite interlayer-like van der Waals bonding. This nanoscale fusing is shown to result in a global densification effect of the carbon nanotube array.

My contribution: Raman and XPS characterization of the samples as well as assistance with paper writing.

Acknowledgments

Every journey eventually comes to an end and so it is time to conclude this chapter of my life with an acknowledgement of the people who supported me in the making of this thesis. First and foremost, I would like to express my gratitude to my supervisor and examiner Johan Liu who once upon a time gave me the opportunity to write my master thesis on thermoelectrics in his lab. Thank you for all the support and trust you have given me over the years. I also wish to thank my co-supervisor Yifeng Fu who always had an open door for valuable discussions regarding research as well as all the help with improving my writing skills. Along this line I also wish to thank Torbjörn Nilsson and Lilei Ye who provided to the academic environment with their expert knowledge and advice.

I would like to thank my current and former colleagues at the packaging group: Di Jiang, Christian Chandra Darmawan, Michael Edwards, Nan Wang, Si Chen, Markus Enmark, Martí Gutierrez Latorre, Wei Mu, Shungxi Sun, Yong Zhang, Nikolaos Logothetis, Nermin Trnjanin, Hafid Zehri, Ya Liu, Oscar Nordin, Aniruddha Paul, Peng Su, Emelie Lindgren, Maulik Satwara, Amos Nkansah, Majid Kabiri Samani and many others for all the encouragement, help and for keeping me company during countless of heated lunch arguments. Thanks to the rest of the Electronics Materials and Systems Laboratory who made friday fika and all the after-work evenings fun.

Special thanks to Josef Hansson who shared the Ph.D. experience with me from the start. You have been a great partner in everything from brainstorming, experiments to equipment maintenance. Thank you for everything, you have been a great colleague and friend over the years.

The work in this thesis would never have been possible without the help from the all-knowing and experienced staff of the cleanroom facility here in the Microtechnology and Nanoscience department. An extra mention goes out to Henric Fjellstedt who has provided excellent IT support to everyone at the department.

This last year has spiced life with uncertainties brought by the Covid-19 pandemic. Therefore, I would like to thank everyone, friends and family, in my life outside work for putting up with me during this time. Thank you, Christin and Thomas, for all the support with childcare which allowed me to fully focus on my writing.

When looking back on the journey that led up to this point, it is important to remember your origins. Therefore, I would like to thank my father Olle Nylander for teaching me many things in life. You once showed me the wonders of science and technology with stories behind nuclear fission and the solid-state transistor. It might not sound like much now but these where pivotal moments that inspired me to continue study and to finally become an academic.

This thesis will, apart from summarizing my time as a Ph.D. student, always serve as a reminder of the first years with my son Benjamin. Seeing how you always try your best, even though life not always agrees, and the glow in your eyes while learning about life has reminded me why I wanted to become a researcher. If you ever read this book I wish you to know that you can do and become anything you set your mind to regardless of what other people might think of you and your potential, that is the real conclusion of this thesis.

The last and most important acknowledgement goes out to my partner in life whom I have shared all best and worst parts of life with. Thank you, Ida, for being the anchor in my life and for helping me become the person I am today. This thesis is dedicated to you.

Andreas Nylander
Göteborg, May 2021

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